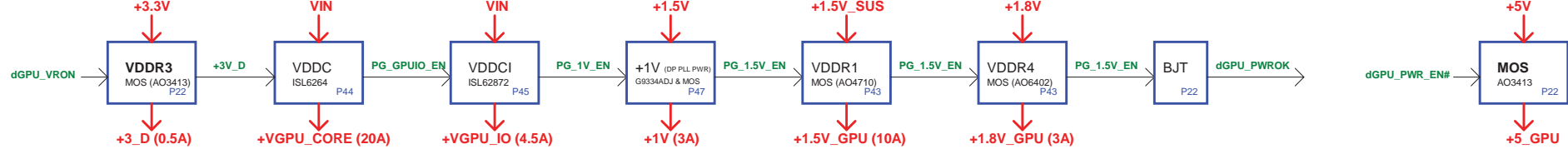
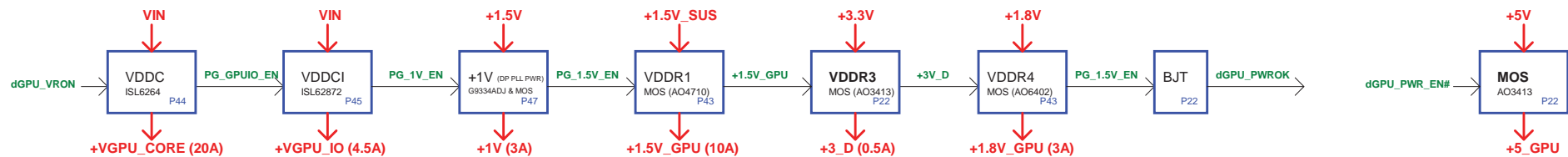


GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



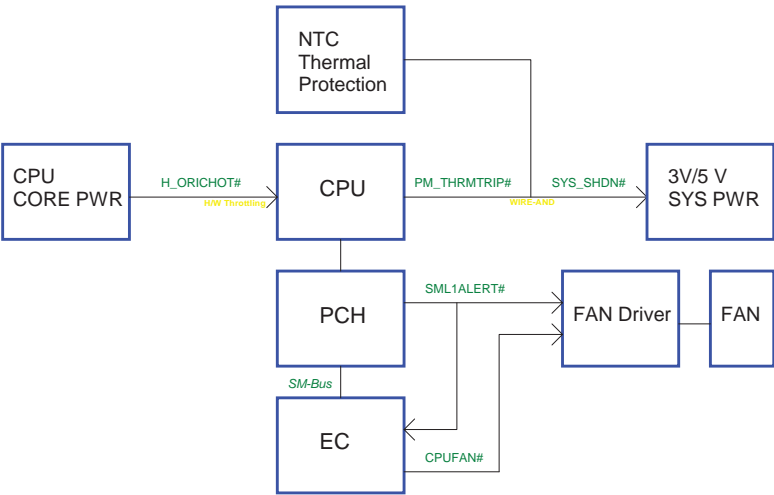
GPU PWR CTRL Option 2 (VDDR3 after VDDR1)

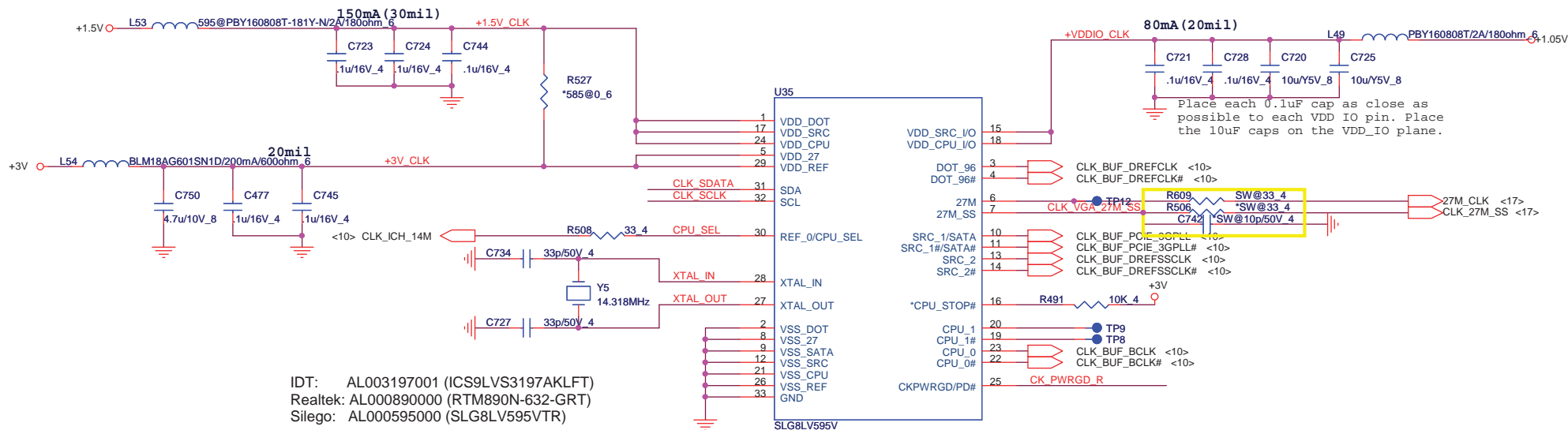


Power States

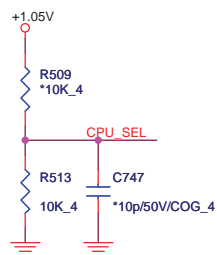
POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	GFX_ON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.1V_VTT	+1.05V or +1.1V	CPU VTT POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+5V_GPU	+5V	SWITCHABLE PWM IC POWER	dGPU_PWR_EN#	Discrete enable
+GPU_CORE	+0.9V~+1.1V	GPU CORE POWER	+3V_D	Discrete enable
+GPU_IO	+0.9V~+1.1V	GPU I/O POWER	PG_GPUIO_EN	Discrete enable
+1.5V_GPU	+1.5V	VRAM CORE POWER	PG_1.5V_EN	Discrete enable
+1.8V_GPU	+1.8V	GPU_CRE/LVDS/PLL POWER	+1.5V_GPU	Discrete enable
+1V	+1V	DP/PEG POWER	PG_1V_EN	Discrete enable

Thermal Follow Chart



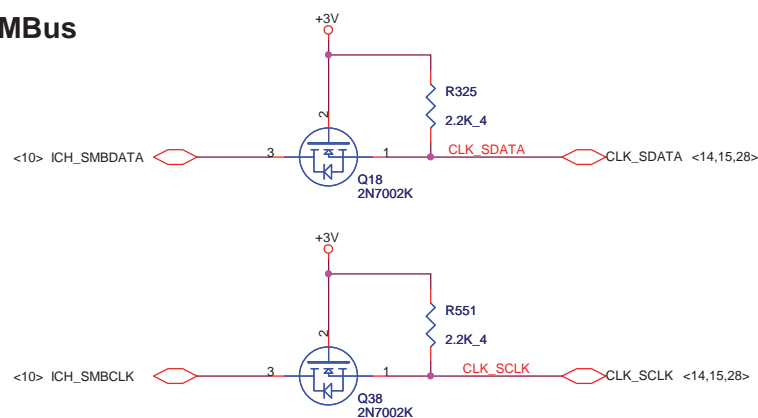


CPU_CLK select

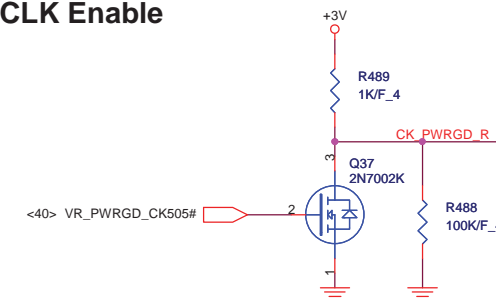


	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

SMBus



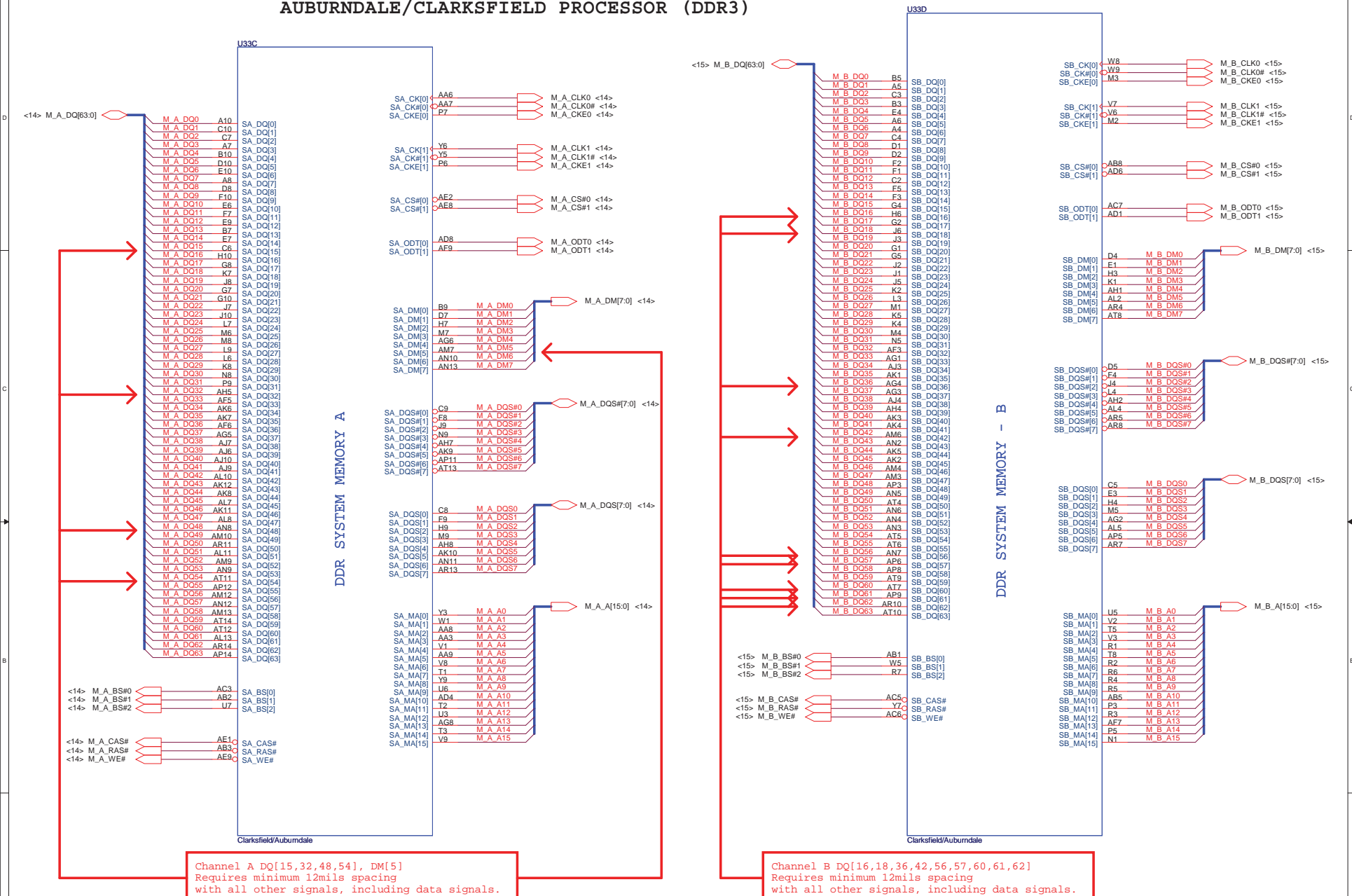
CLK Enable

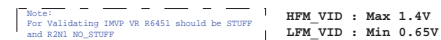


Quanta Computer Inc.
PROJECT : ZR7B

Size	Document Number	Rev
	Clock Generator	1A
Date:	Friday, March 05, 2010	Sheet 3 of 50

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

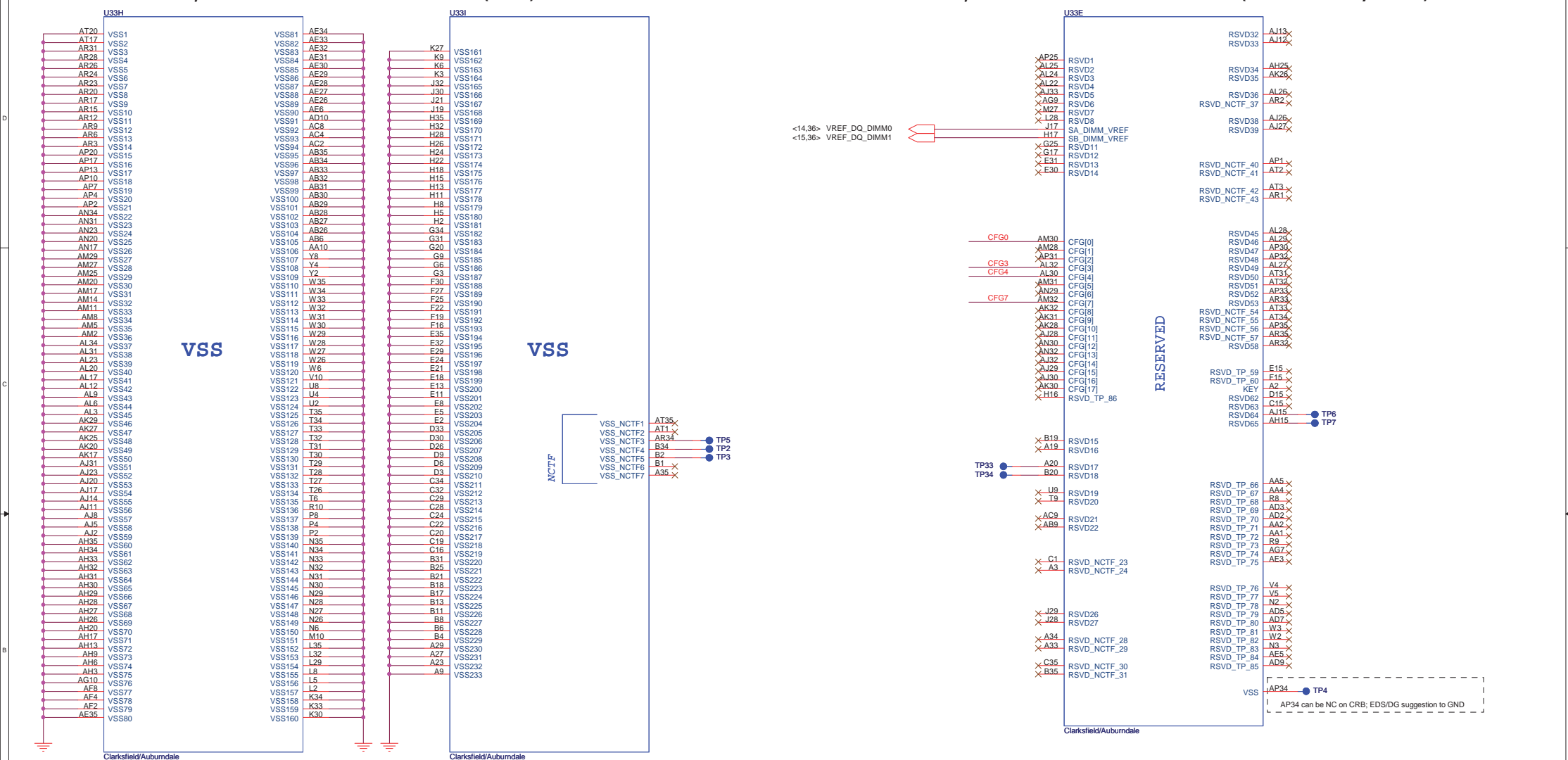




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AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

AUBURNDALE/CLARKSFIELD PROCESSOR (RESERVED, CFG)

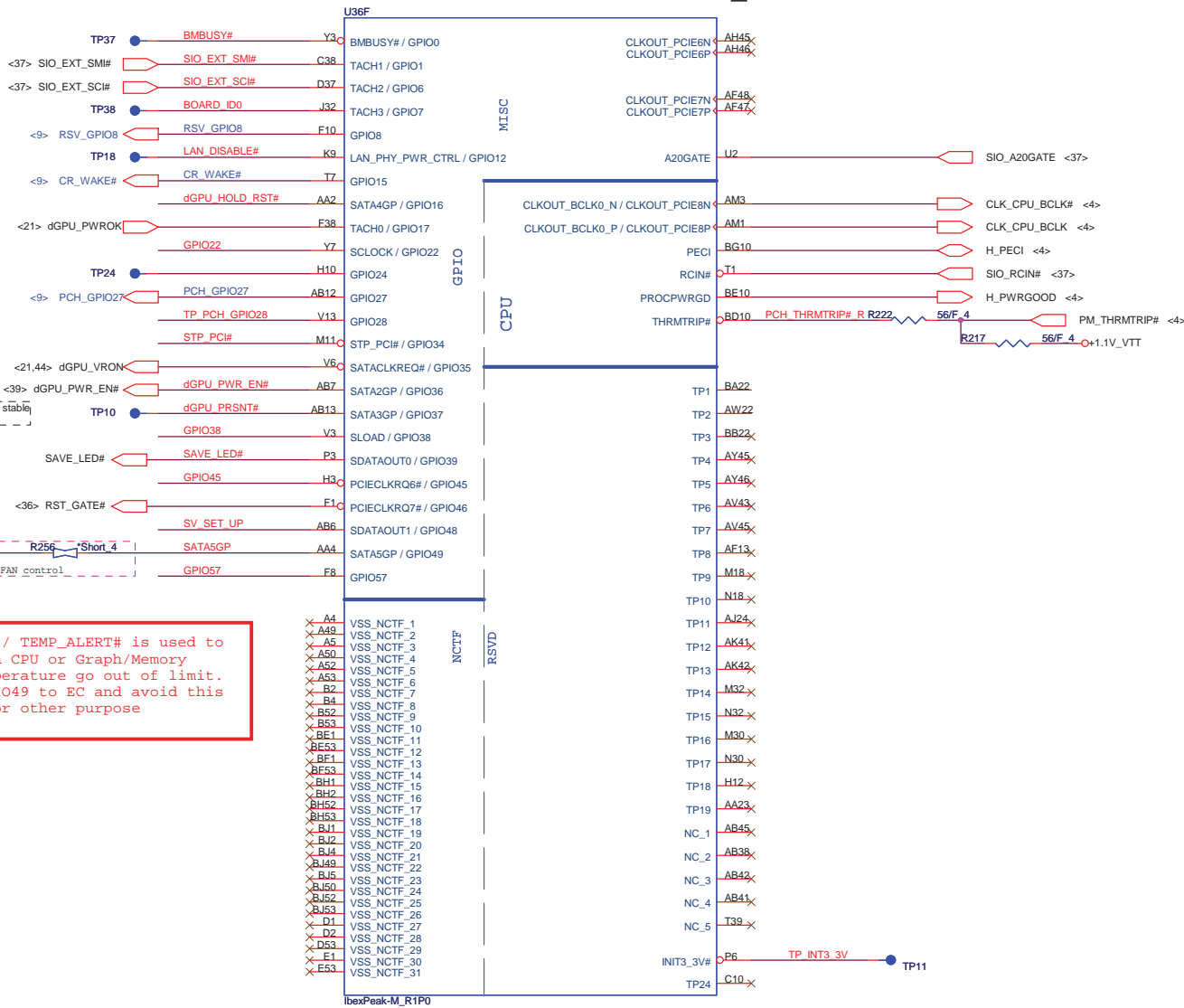


Processor Strapping

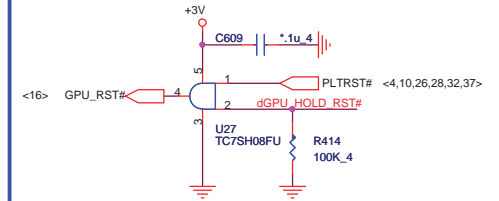
	1	0	DEFAULT	
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled	1	CFG0 R186 ~3.01K NC
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed	1	CFG3 R169 ~3.01K/F_4
CFG4 (Embedded Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port	1	CFG4 R162 ~3.01K
T h b e t p B A				CFG7 R172 ~3.01K/F_4



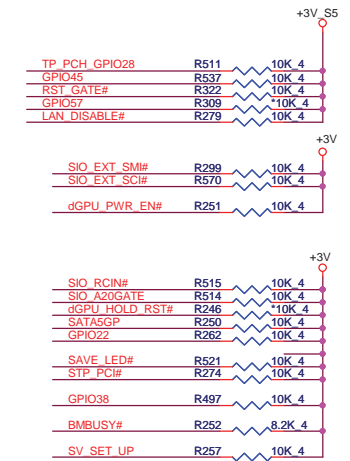
IBEX PEAK-M (GPIO, VSS_NCTF, RSVD)



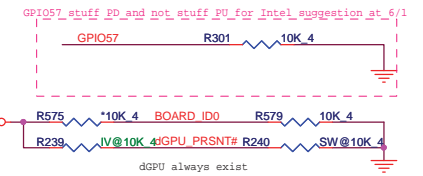
GPU RST#



GPIO Pull-up/Pull-down



SV_SET_UP	1-X High = Strong (Default)
-----------	-----------------------------

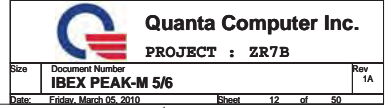


BOARD_ID0	High = JV41/JM41 Low = JM51
RSV_GPIO8	High = Disable Low = Enable

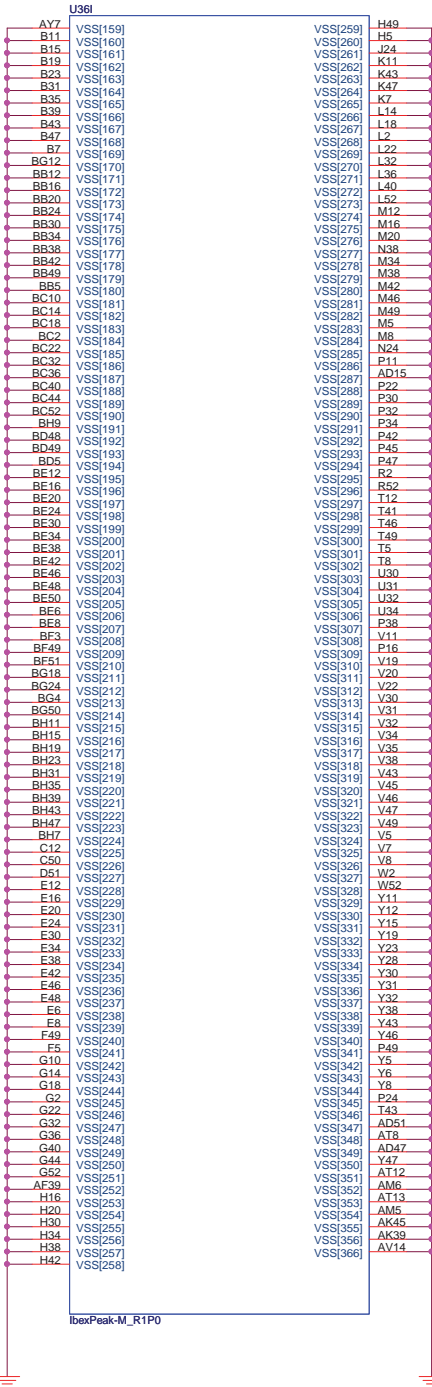
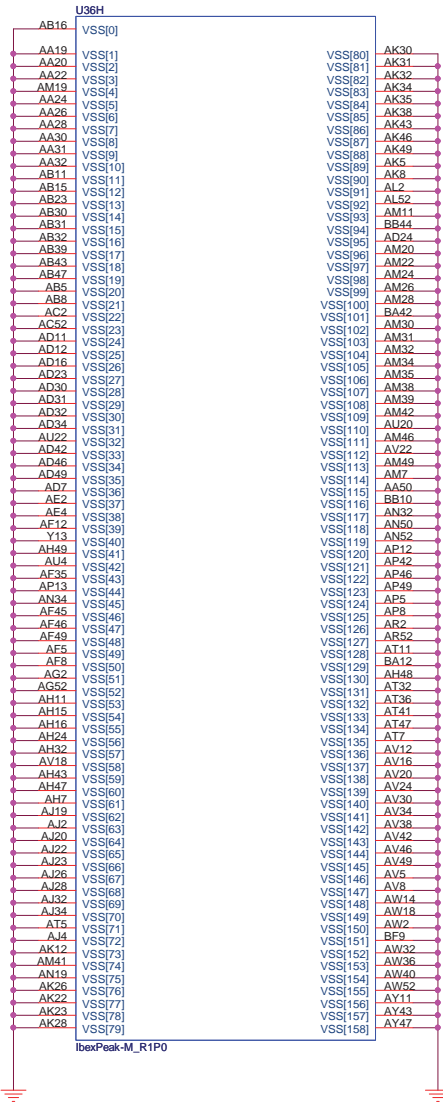


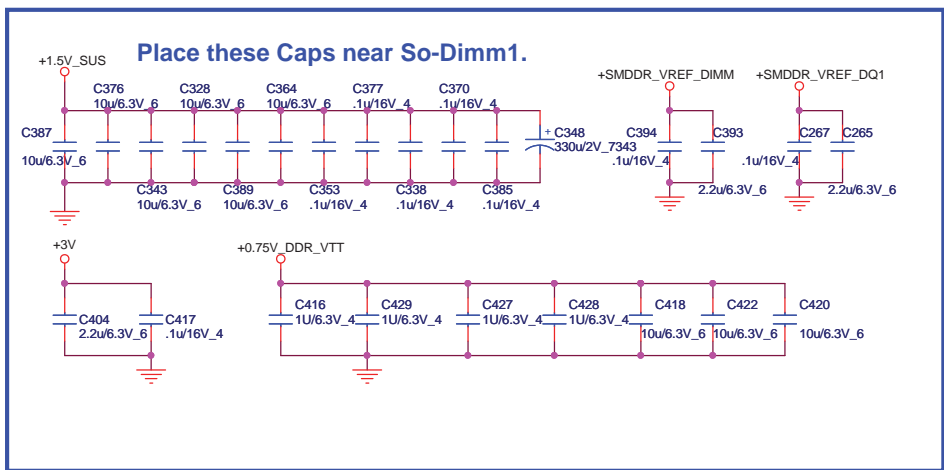
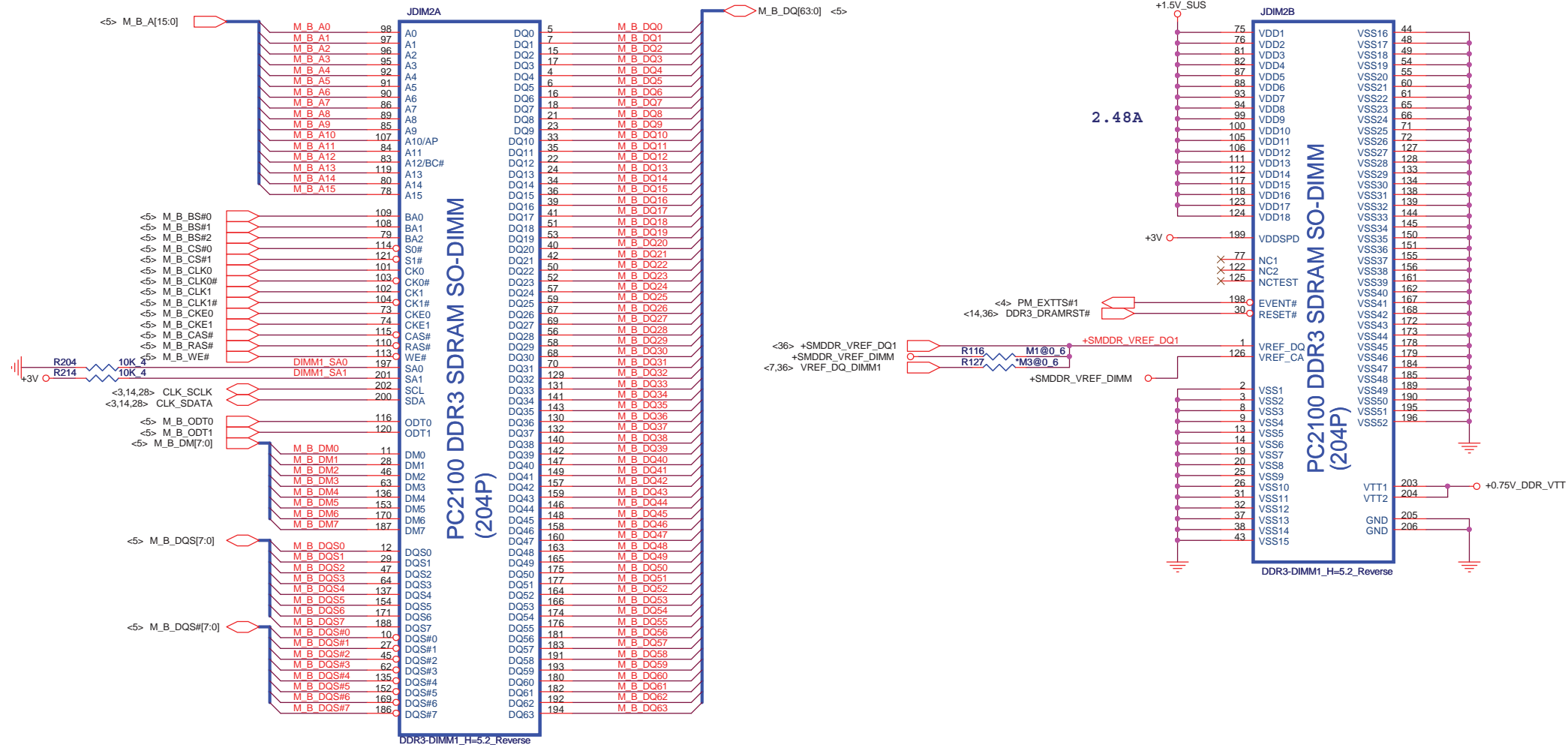
Quanta Computer Inc.
PROJECT : ZR7B

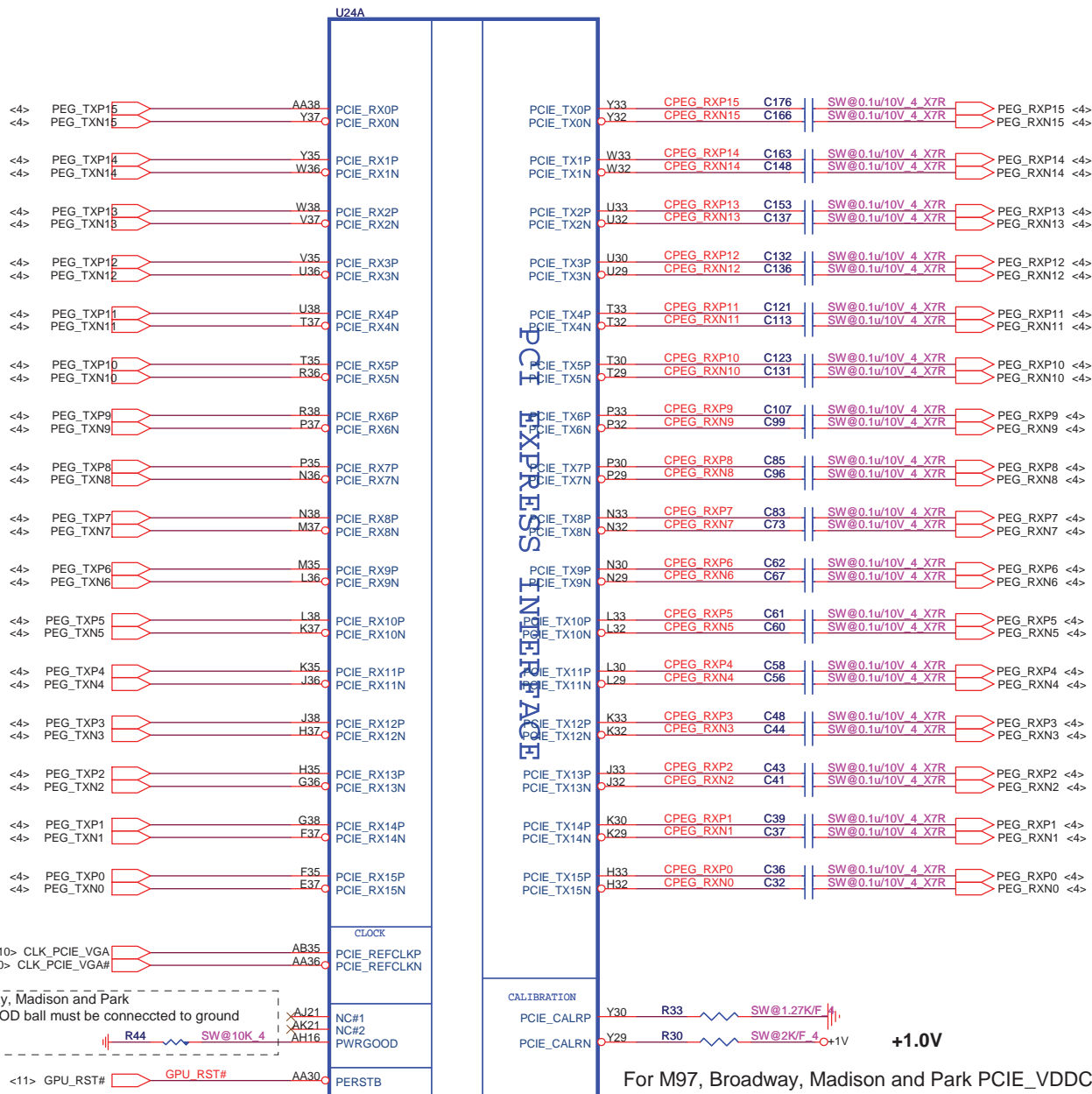
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IBEX PEAK-M (GND)



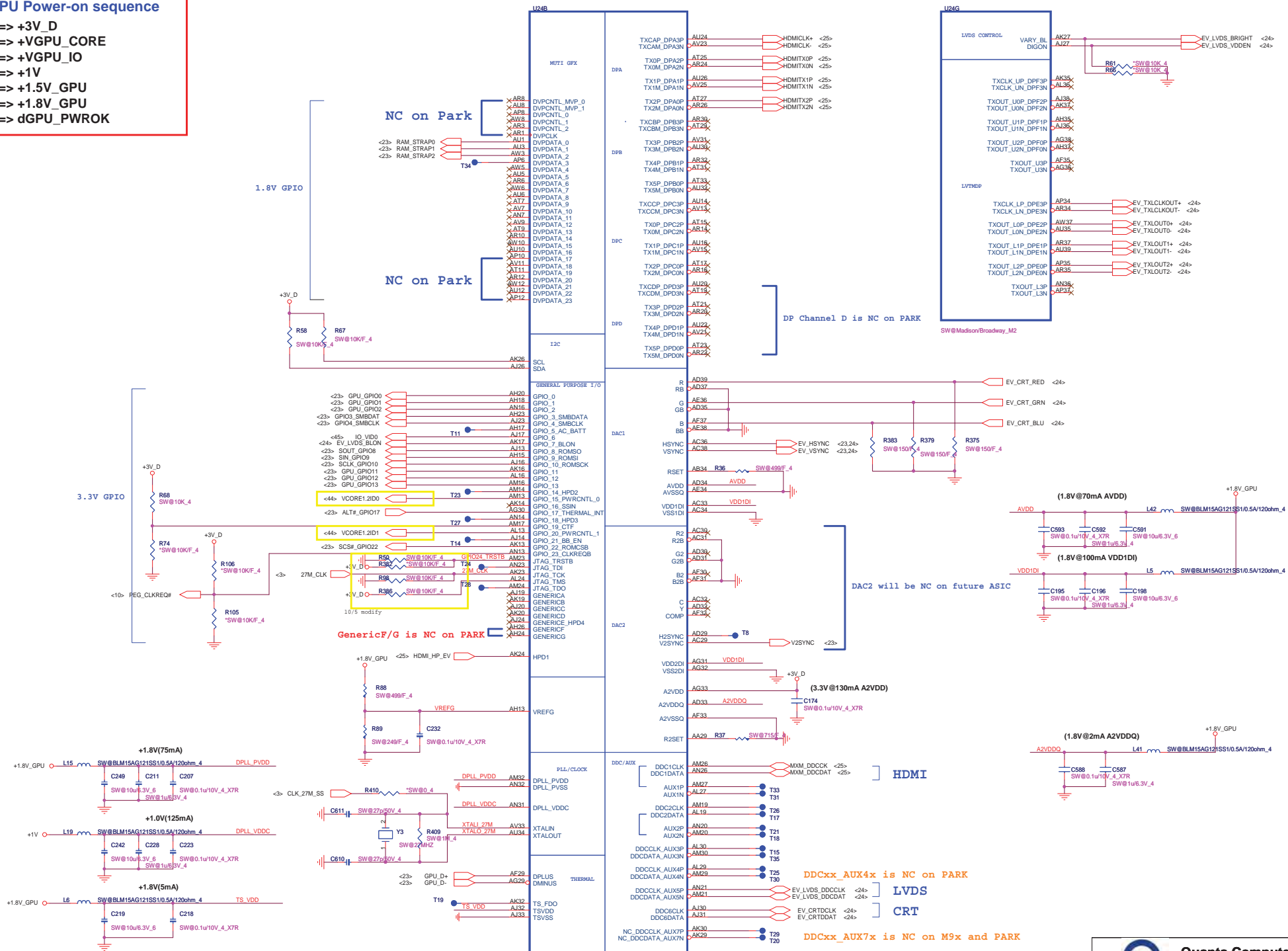




Quanta Computer Inc.
PROJECT : ZR7B

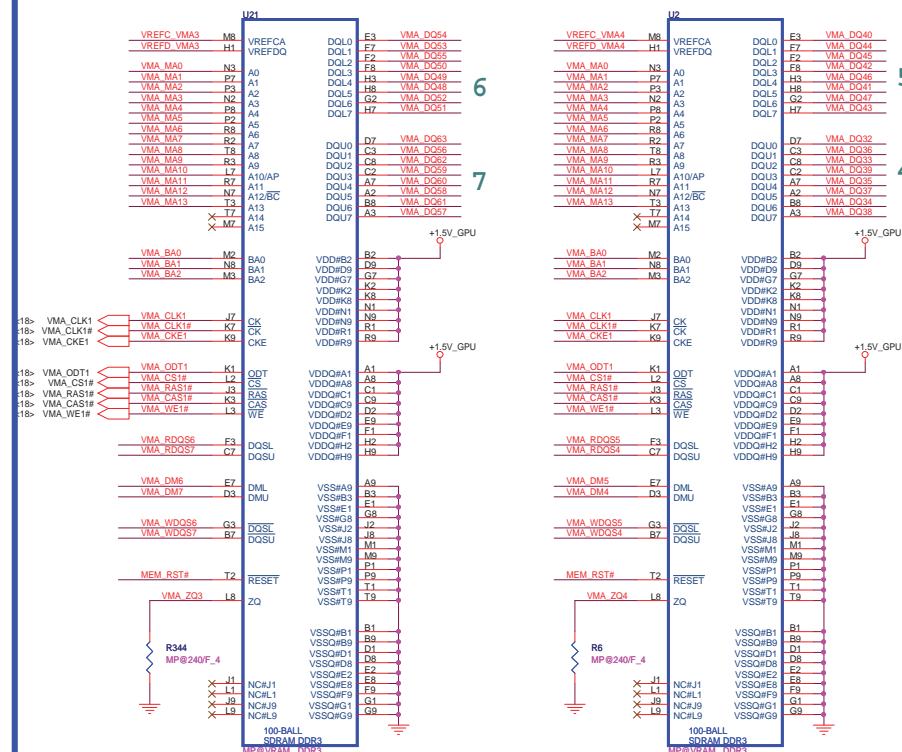
Size	Document Number	Rev 1A
Madison/Broadway-PCIE I/F		
Date:	Friday, March 05, 2010	Sheet 16 of 50

1 => +3V_D
2 => +VGPU_CORE
3 => +VGPU_IO
4 => +1V
5 => +1.5V_GPU
6 => +1.8V_GPU
7 => dGPU_PWROK





Park, M92M Use Channel B Memory Interface Only

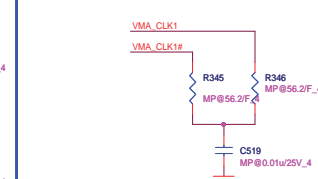
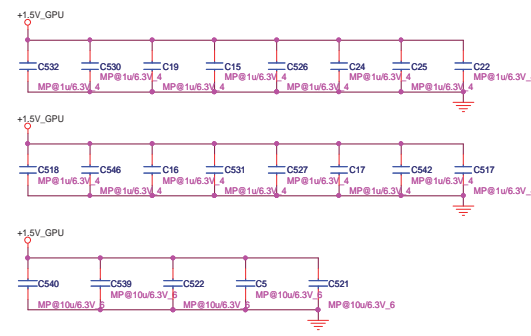


TOP Right

Group-A1 VREF



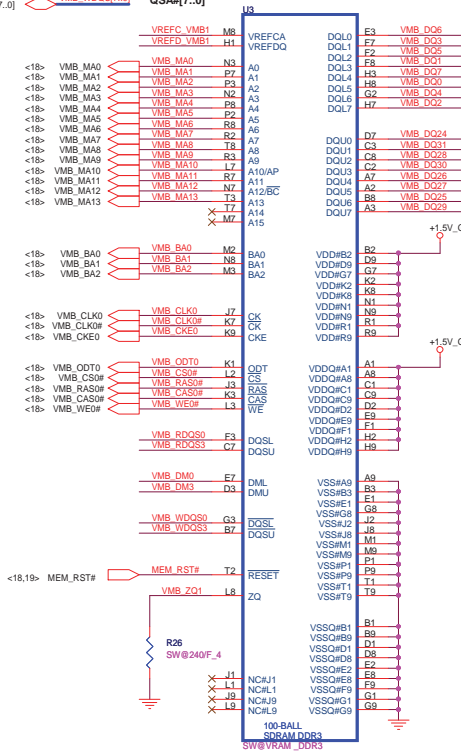
MEM_A1 CLK



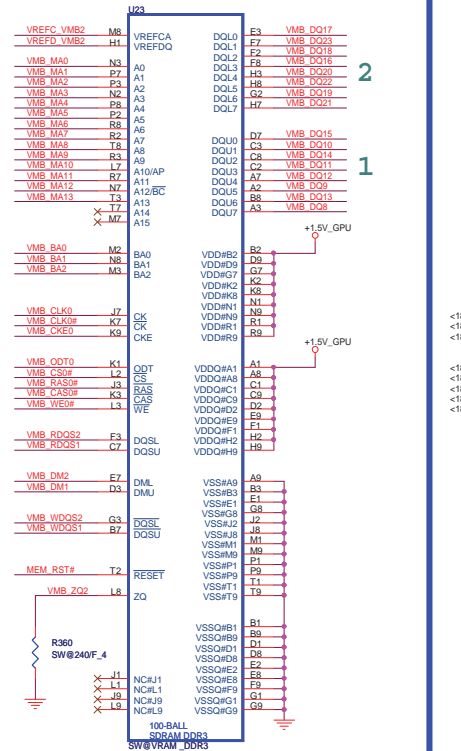
CHANNEL B: 512MB DDR3 (64M*16*4pcs)

<18> VMB_DQ[63..0]
<18> VMB_DM[7..0]
<18> VMB_RDSQ[7..0]
<18> VMB_WDQS[7..0]

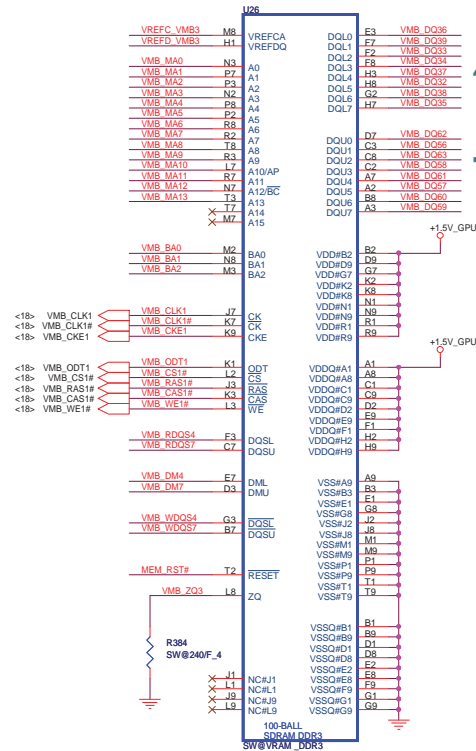
QSA[7..0]
QSA# [7..0]



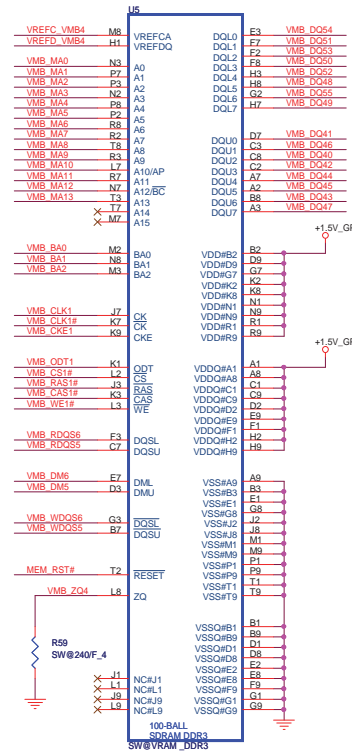
BOT Down



TOP Down

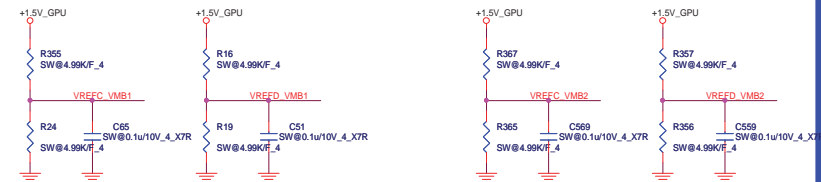


TOP Up

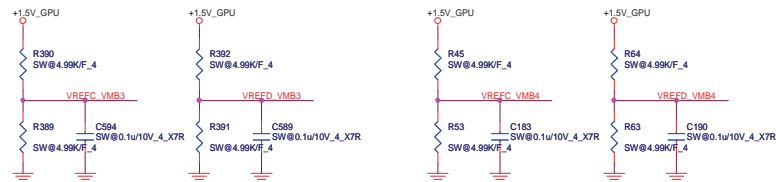


BOT Up

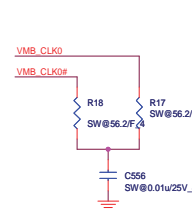
Group-B0 VREF



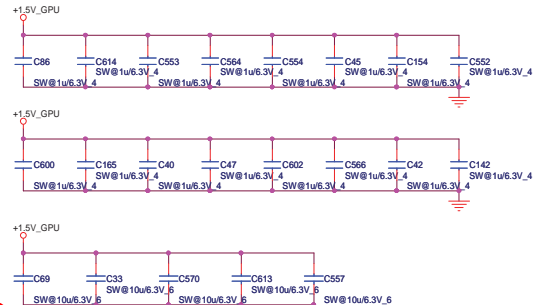
Group-B1 VREF



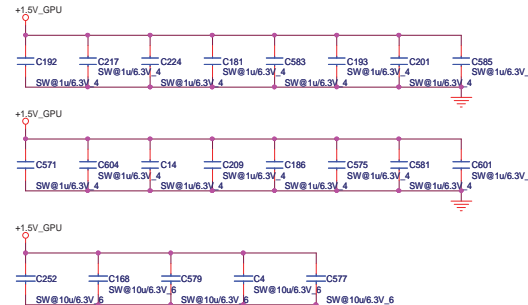
MEM_B0 CLK



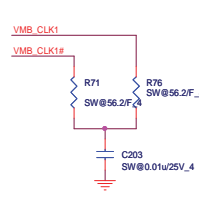
Group-B0 decoupling CAP



Group-B1 decoupling CAP



MEM_B1 CLK



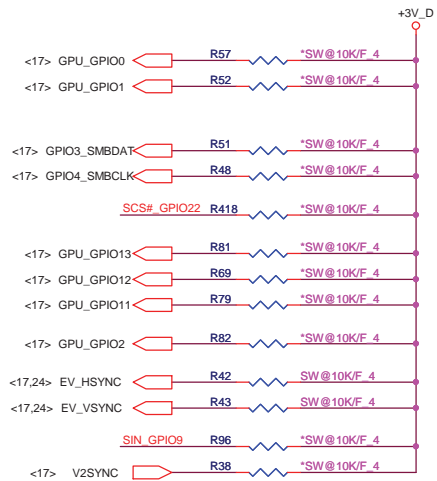
Quanta Computer Inc.

PROJECT : ZR7B

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Rev 1A

PIN STRAPS



Memory Aperture size	
GPIO[13:11]	Size
000	128MB
001	256MB
010	64MB
011	32MB

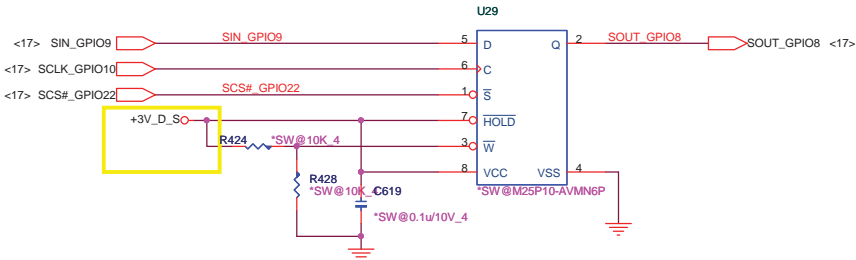
ROM Table		
EXT_HSYNC	EXT_VSYNC	Discription
0	0	No Audio
0	1	Any one by dectec
1	0	DP only
1	1	Both DP & HDMI

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0 = DISABLE 1 = ENABLE	0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT NUMONYX M25P10A : 101	000	See Memory Aperture size
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

EEPROM



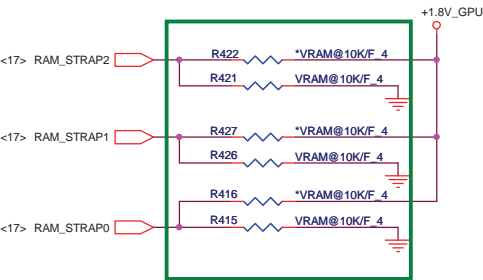
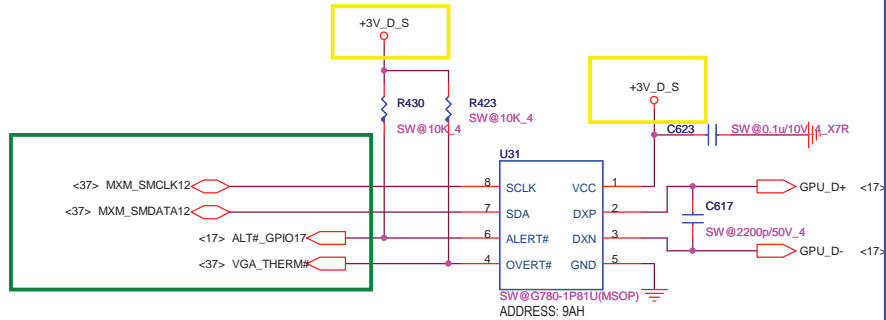
DDR3 Memory Aperture size

DDR3 Memory Aperture size

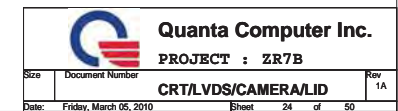
Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Hynix	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	512MB	1	1	0
			1GB	1	0	0
			2GB	1	0	1
Samsung	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	512MB			
			1GB	0	0	0
AMD	K4W2G1646B-HC12	AKD5MGGT500	2GB	0	0	1
	23EY2387MA12-SZ	AKD5LGGT700	1GB	0	1	0

Thermal Sensor

NS	none
WINDBOND	AL83L771K02
GMT	AL000780003

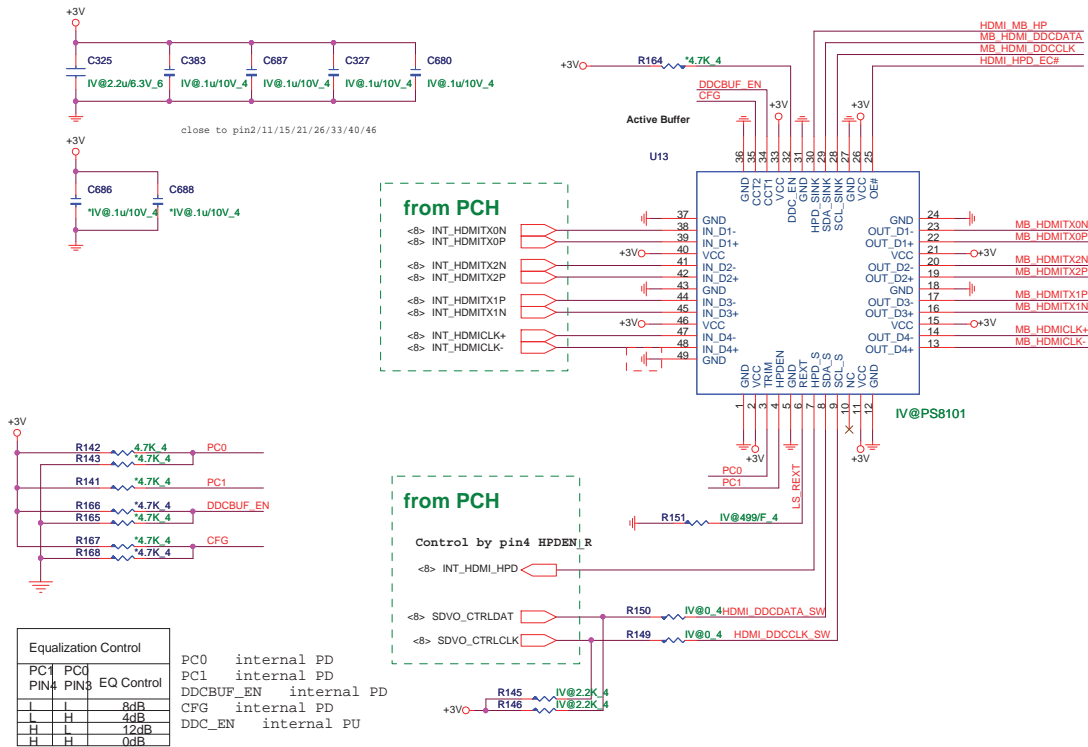


RAM_STRAP2 SET DDR3 Vendor
RAM_STRAP[1:0] SET SIZE.

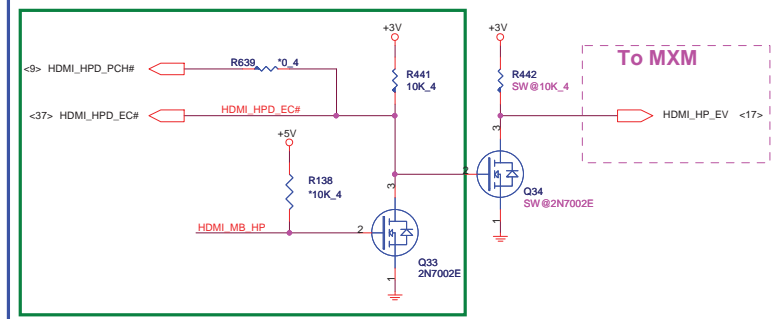
IV@
SW@

I@ HDMI LEVEL SHIFTER

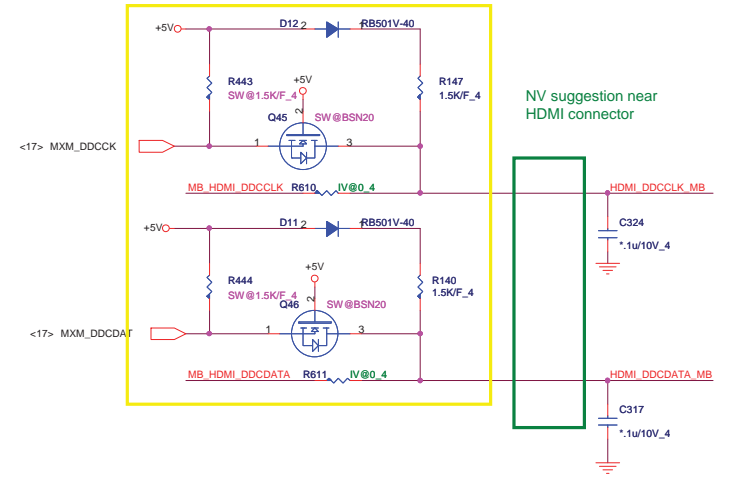
IV@
SW@
SP@



SW@HDMI-detect

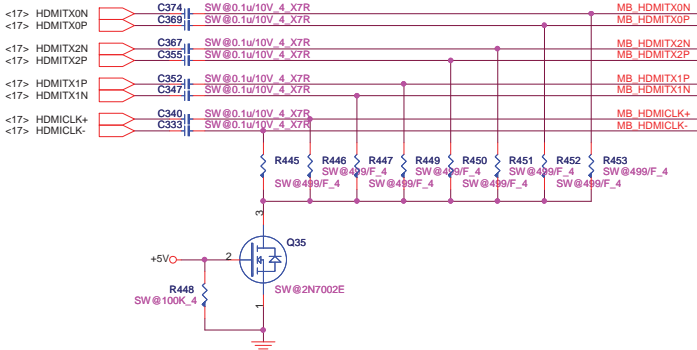


I2C

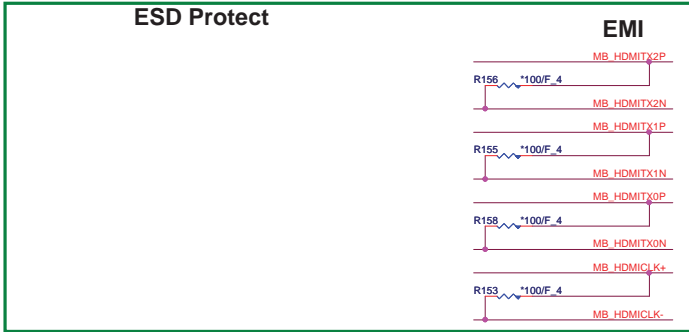


Switchable Graphic HDMI source

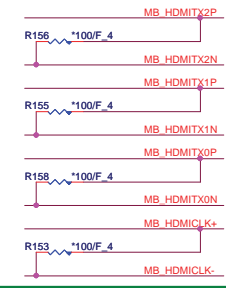
To MXM



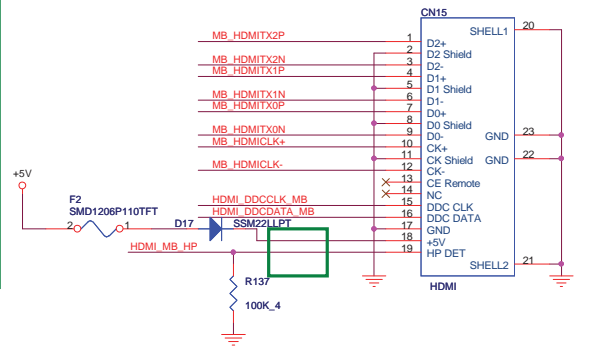
ESD Protect



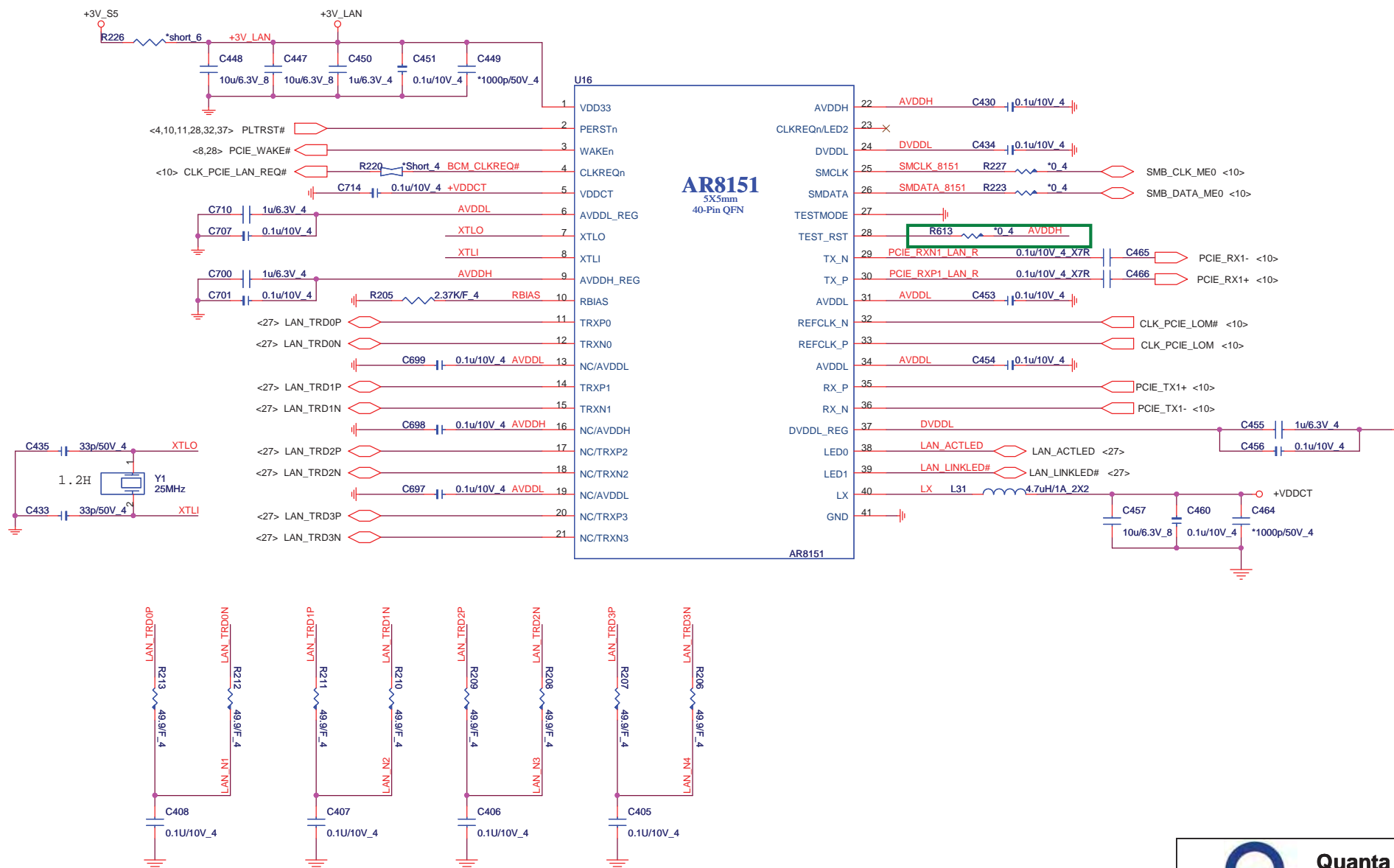
EMI

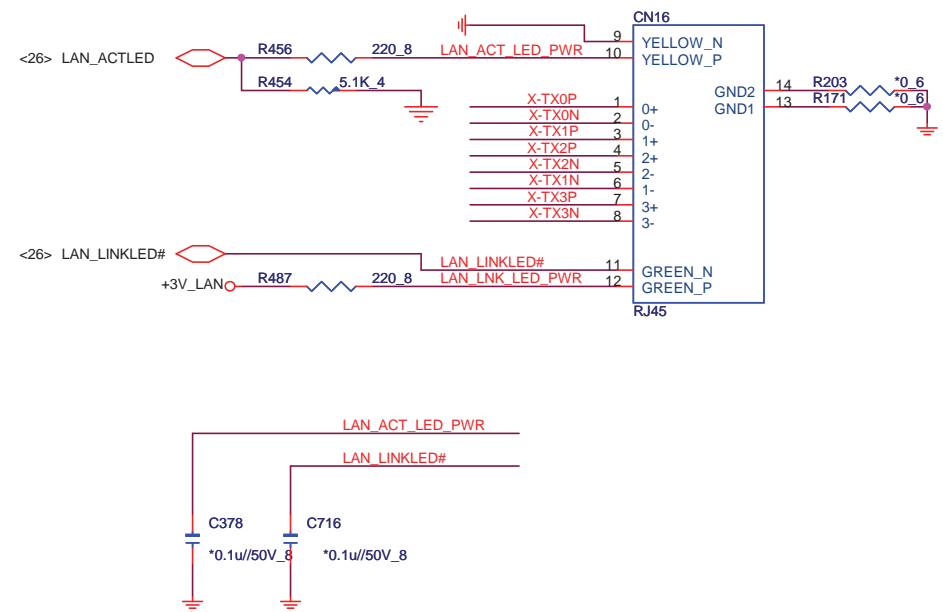
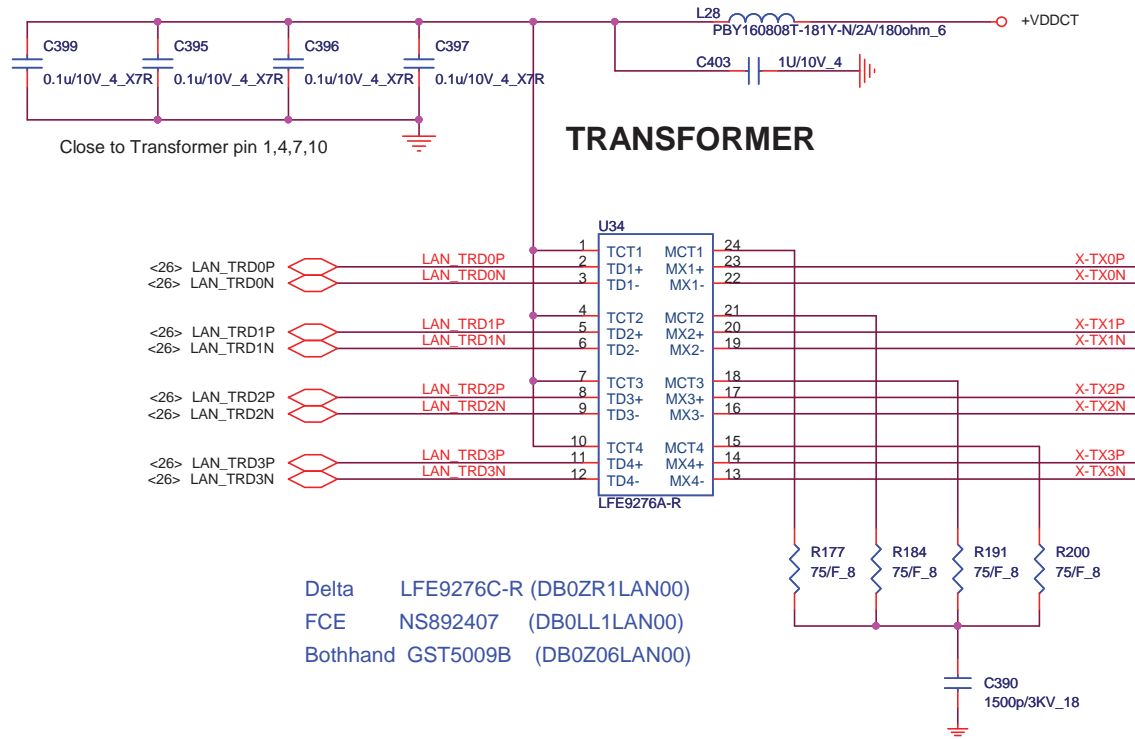


HDMI connector



Giga-LAN AR8151





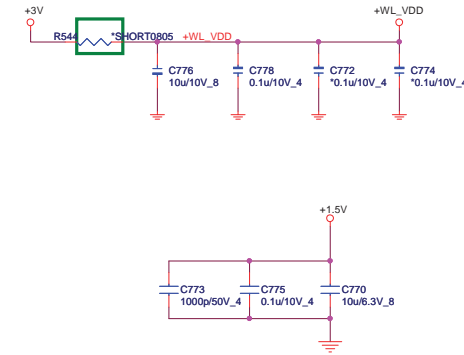
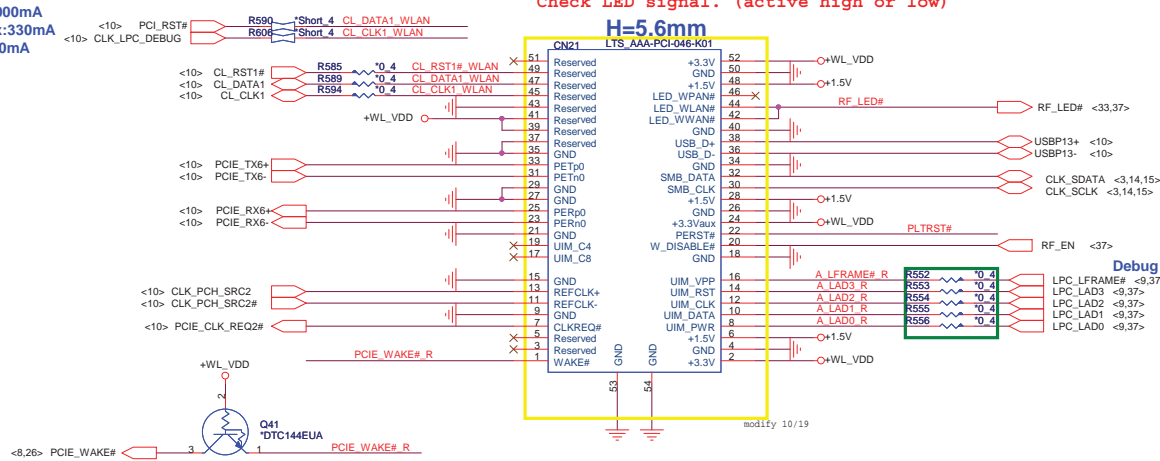
MINI-CARD WLAN(MPC)

+3.3V:1000mA
+3.3Vaux:330mA
+1.5V:500mA

Check LED signal. (active high or low)

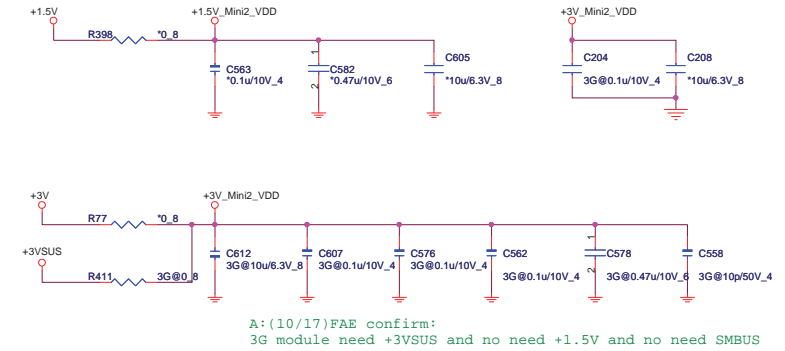
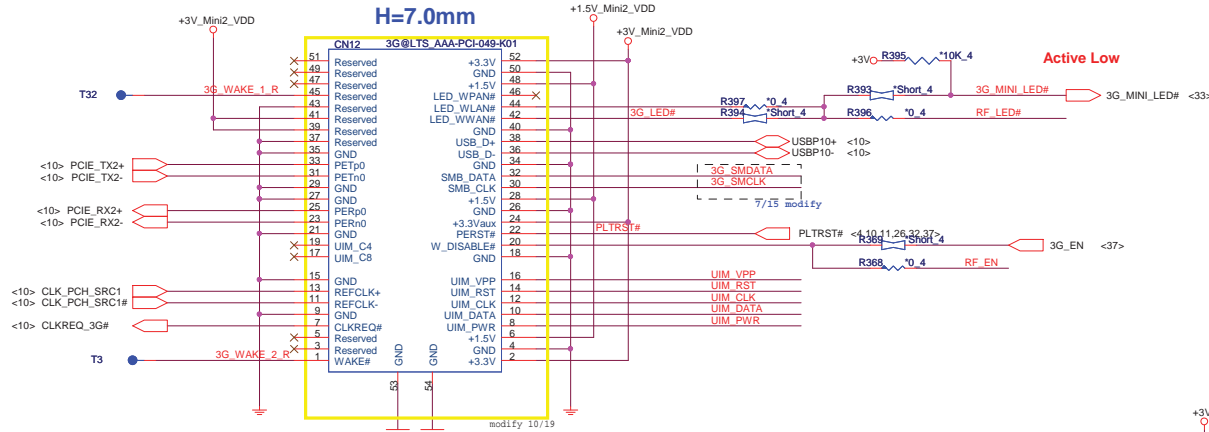
H=5.6mm

LTS AAA-PCI-046-K01



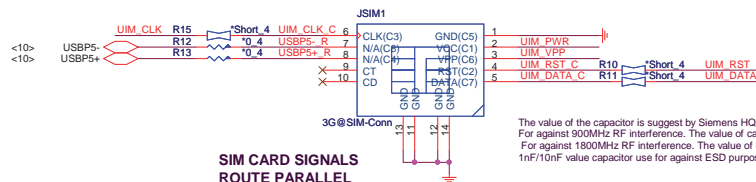
MINI-CARD 3G(MNC)Reserve for JV41-CP

H=7.0mm



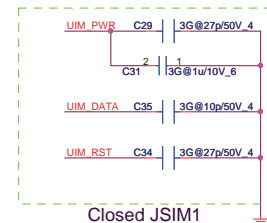
A:(10/17)FAE confirm:
3G module need +3VSUS and no need +1.5V and no need SMBUS

SIM CARD(RFM)Reserve for JV41-CP

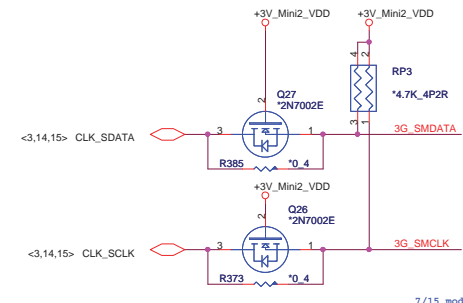


SIM CARD SIGNALS
ROUTE PARALLEL

The value of the capacitor is suggest by Siemens HQ expert.
For against 900MHz RF interference. The value of capacitor is 27pF.
For against 1800MHz RF interference. The value of capacitor is 10pF.
1nF/10nF value capacitor use for against ESD purpose.



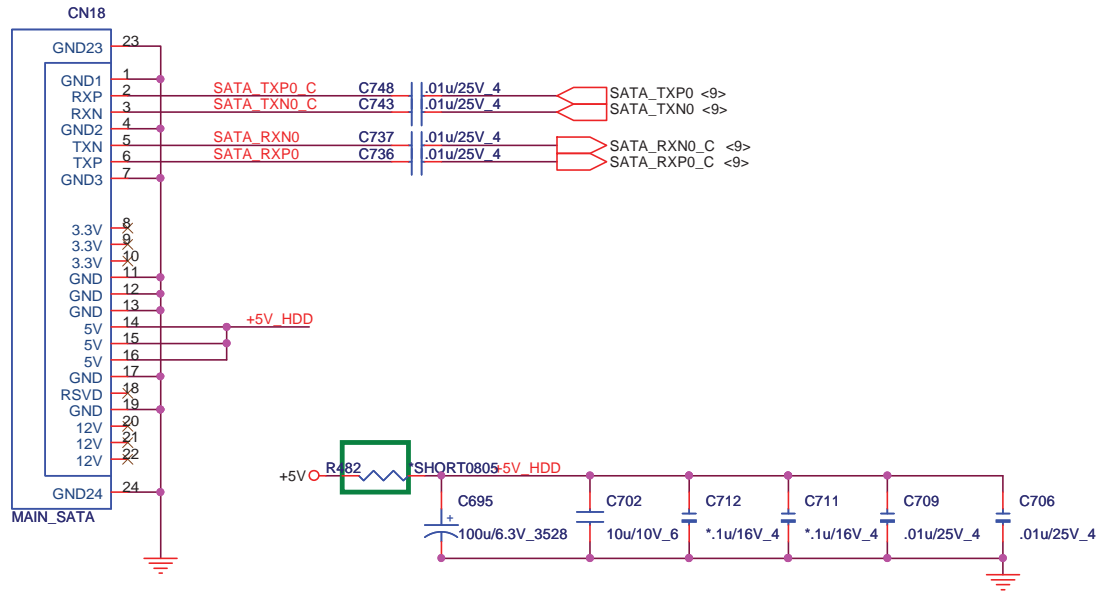
Closed JSIM1



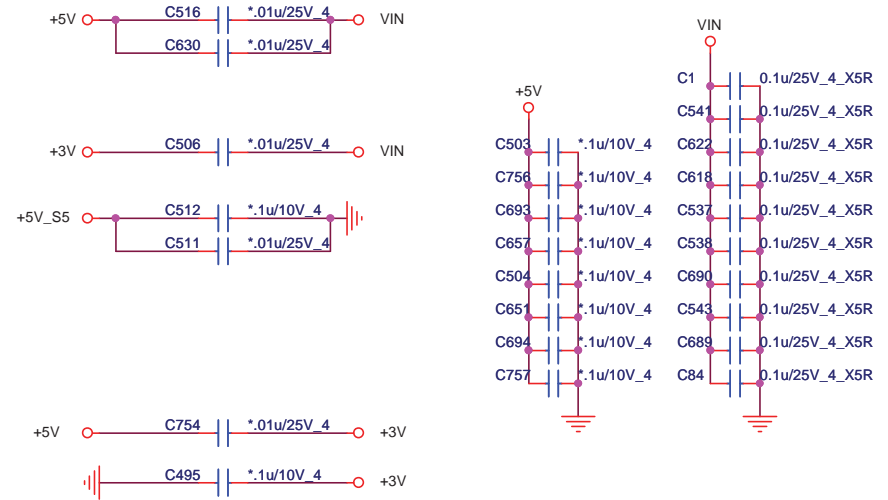
Quanta Computer Inc.
PROJECT : ZR7B

Size	Document Number	Rev
	MINI PCI-E card/TV	1A
Date:	Friday, March 05, 2010	Sheet 28 of 50

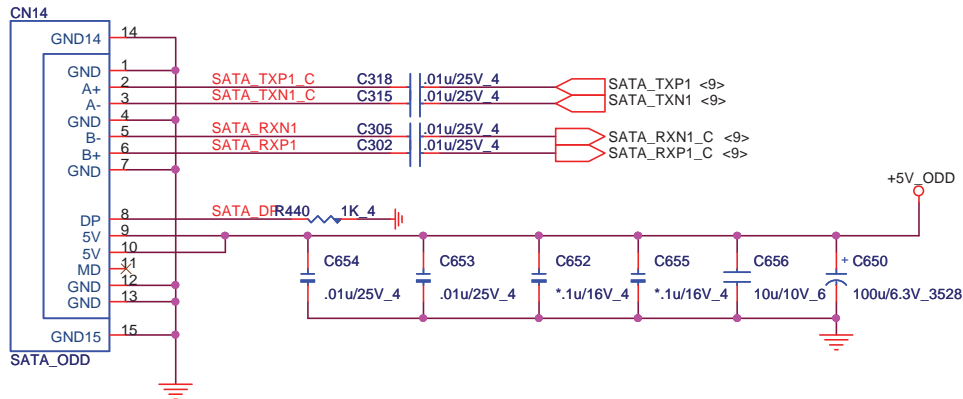
MAIN SATA HDD



EE RETURN-PATH CAPACITORS

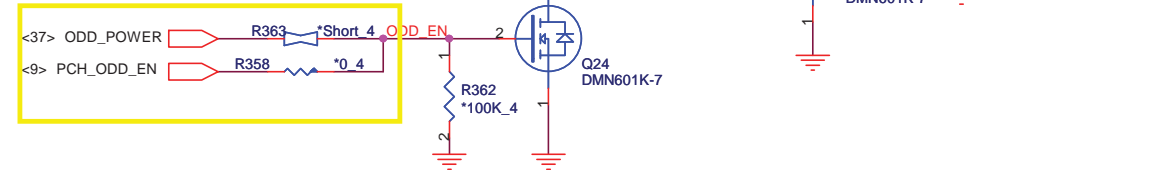


ODD (SATA)



ODD POWER(ODD)

Connect to PCH(GPIO21) pin Y9
and EC pin28(GPIO53)



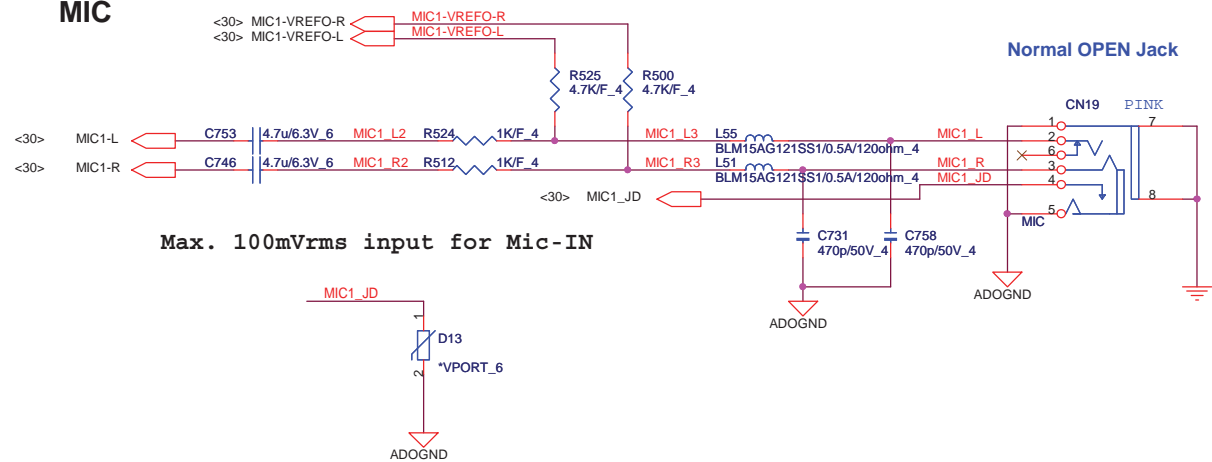
Quanta Computer Inc.

PROJECT : ZR7B

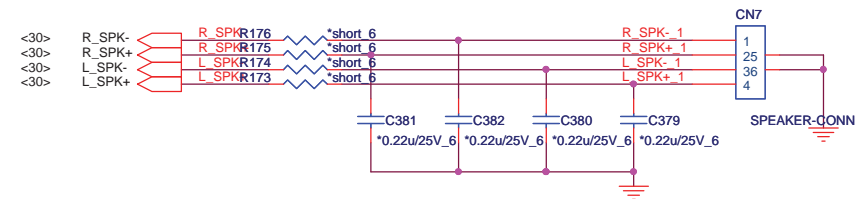
Size	Document Number	Rev
	SATA-HDD/ODD/USB-ESATA	1A

Date: Friday, March 05, 2010 Sheet 29 of 50

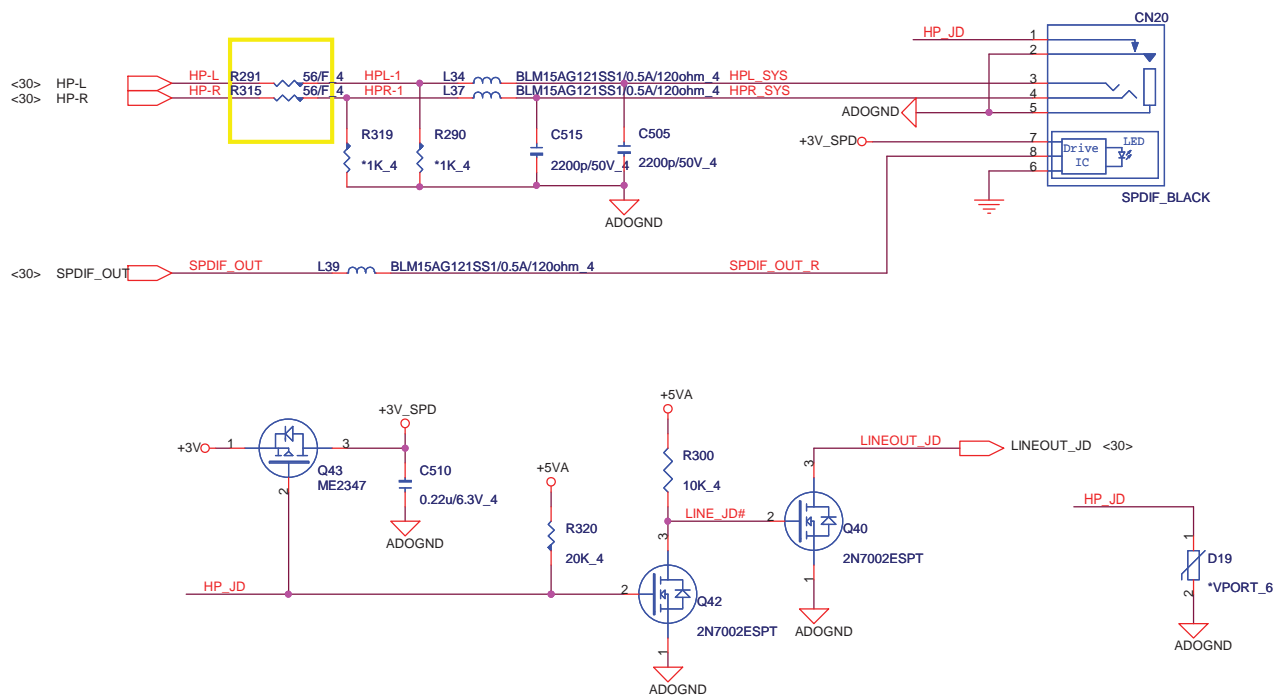
MIC



Internal Speaker



HP/SPDIF

**Quanta Computer Inc.**

PROJECT : ZR7B

AMP /AUDIO JACK CONN

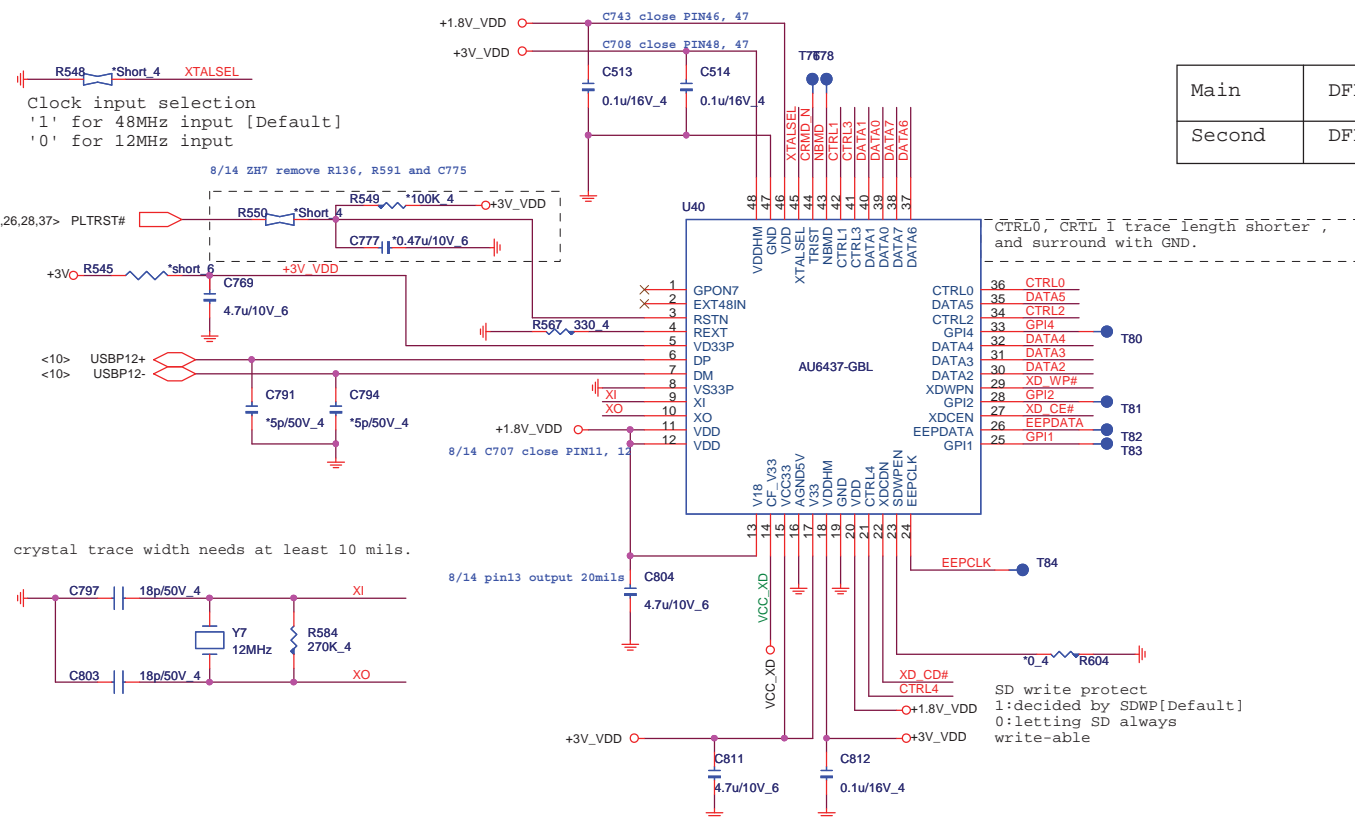
Size	Document Number
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Date: Friday, March 05, 2010

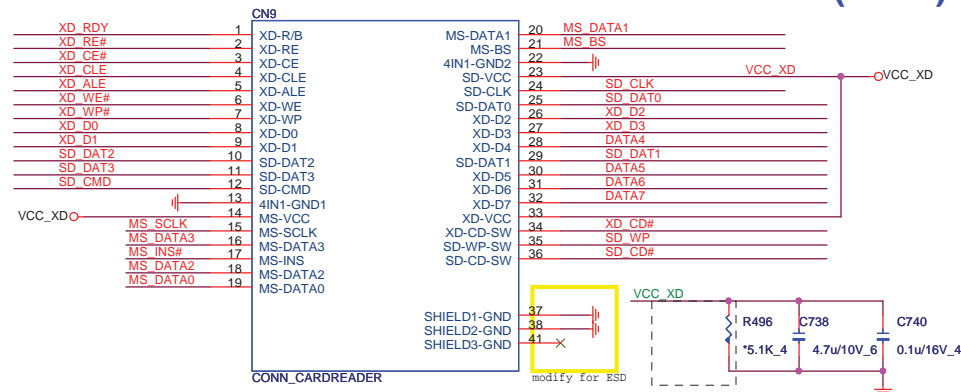
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CARD READER Controller

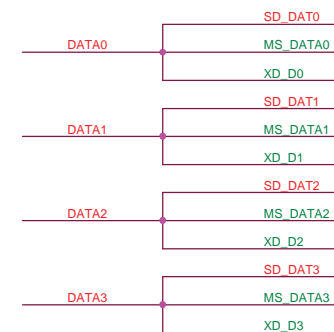


4 IN 1 CARD READER (MMC)

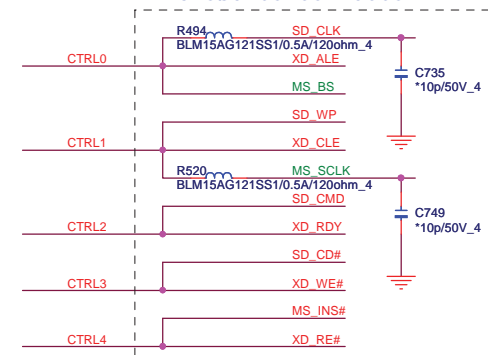


Close to CN14 pin 14 & pin23
4.7u CAP close to pin23

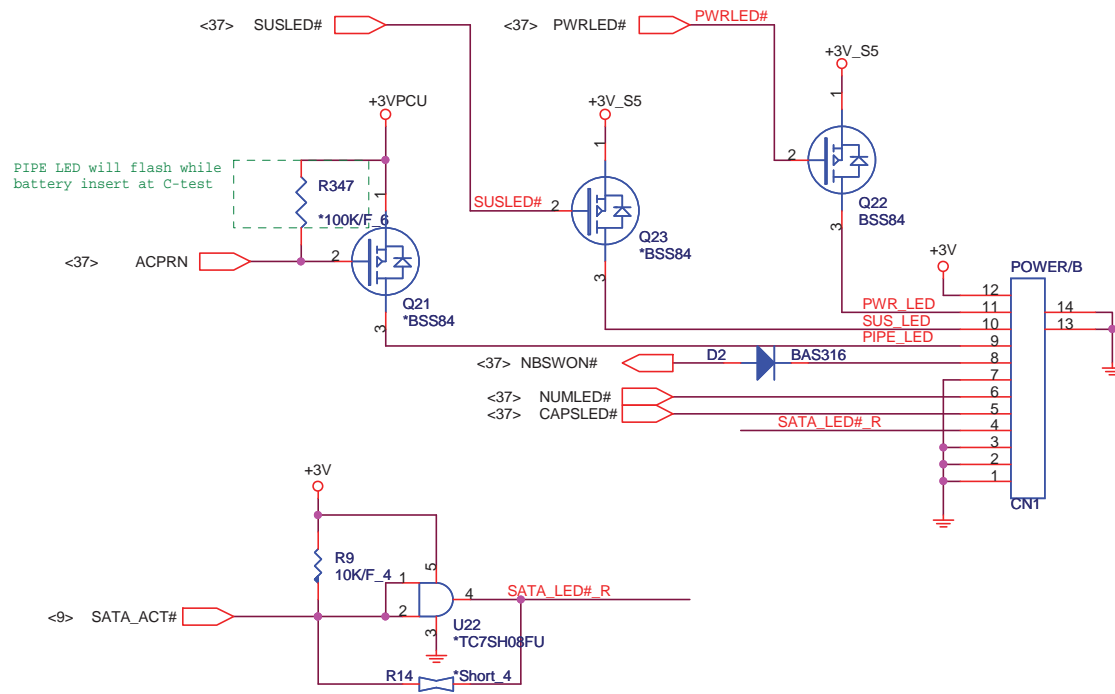
Main	DFHD36MS006
Second	DFHD36MS012



Close to connector

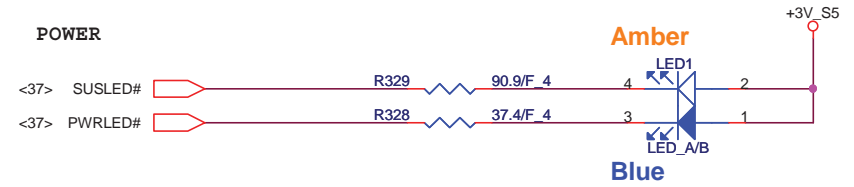


POWER BOARD CONN(UIF)

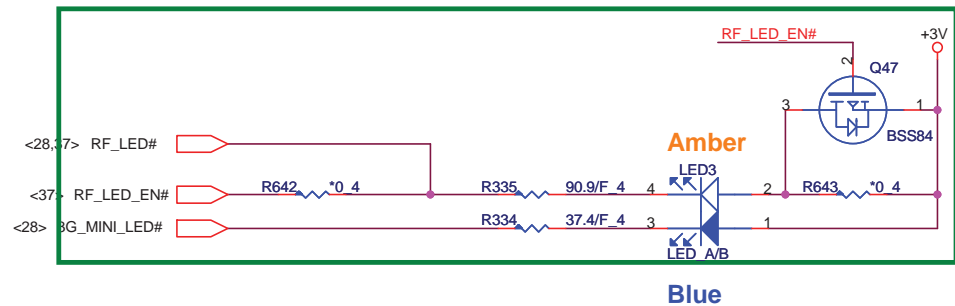
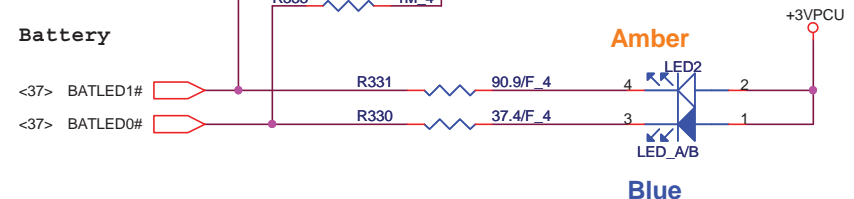


LED

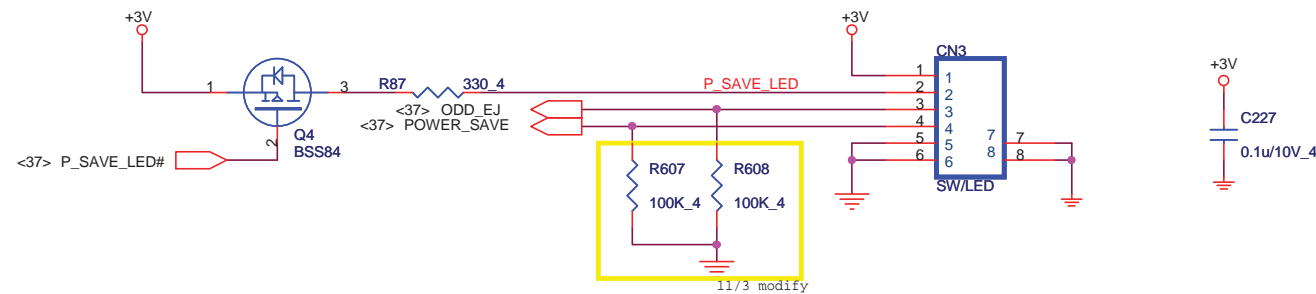
POWER




Battery

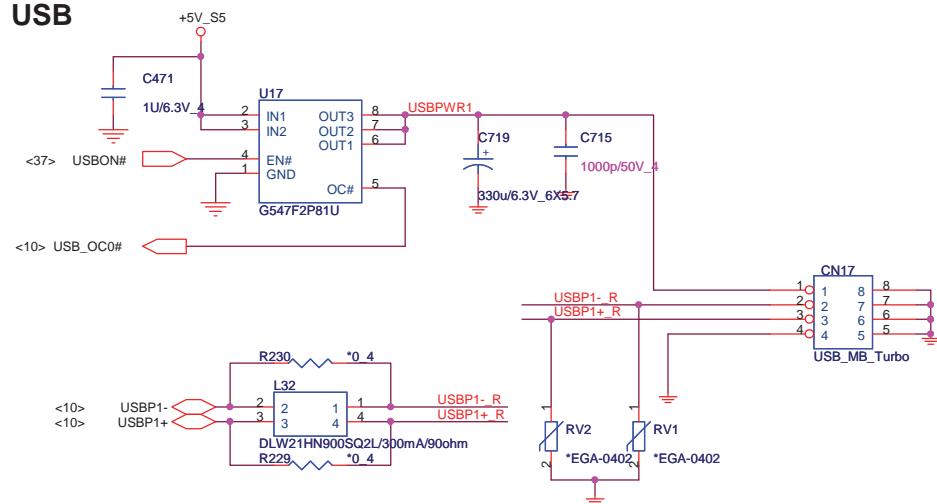


SW /B

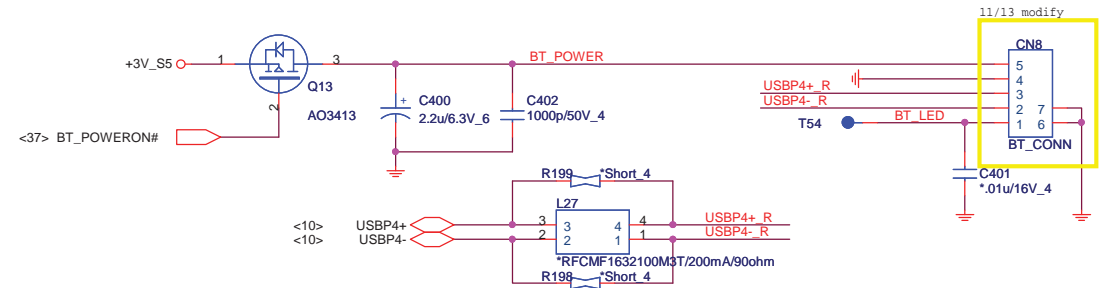


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		POWER/MMB/LAUNCH/LED		
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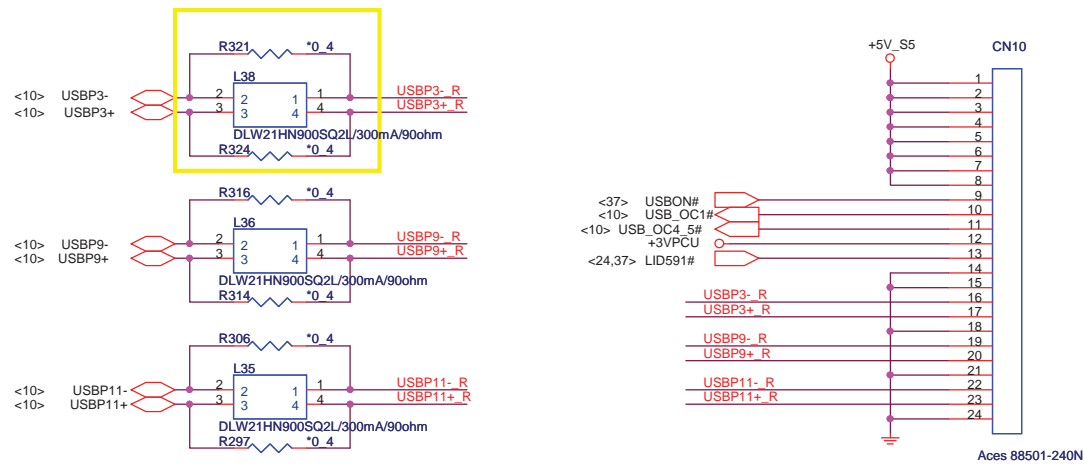
USB




BLUETOOTH CONNECTOR

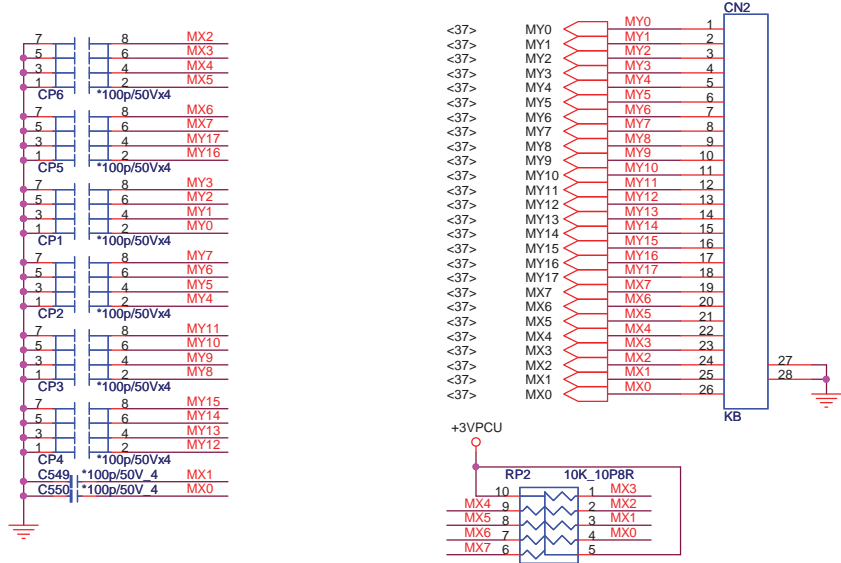


USB/B

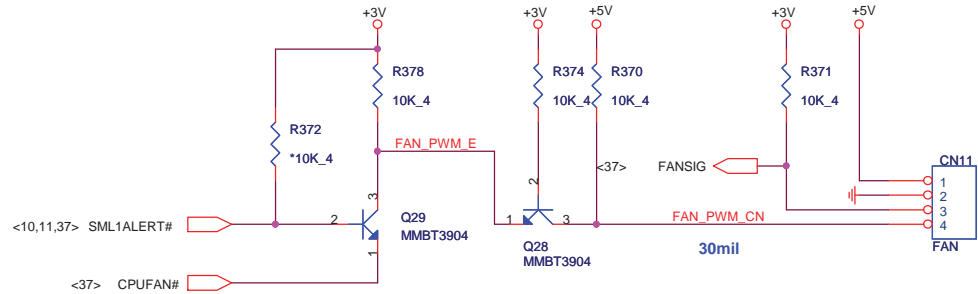


R230, R229, R321, R324, R316, R314, R306, R297

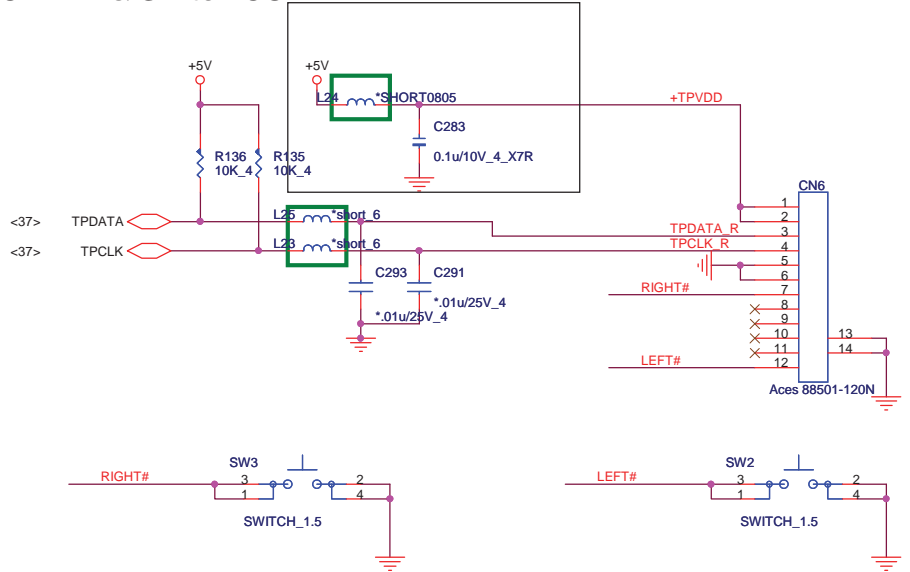
 Quanta Computer Inc. PROJECT : ZR7B		Rev
		1A
Size	Document Number	USB/ BT
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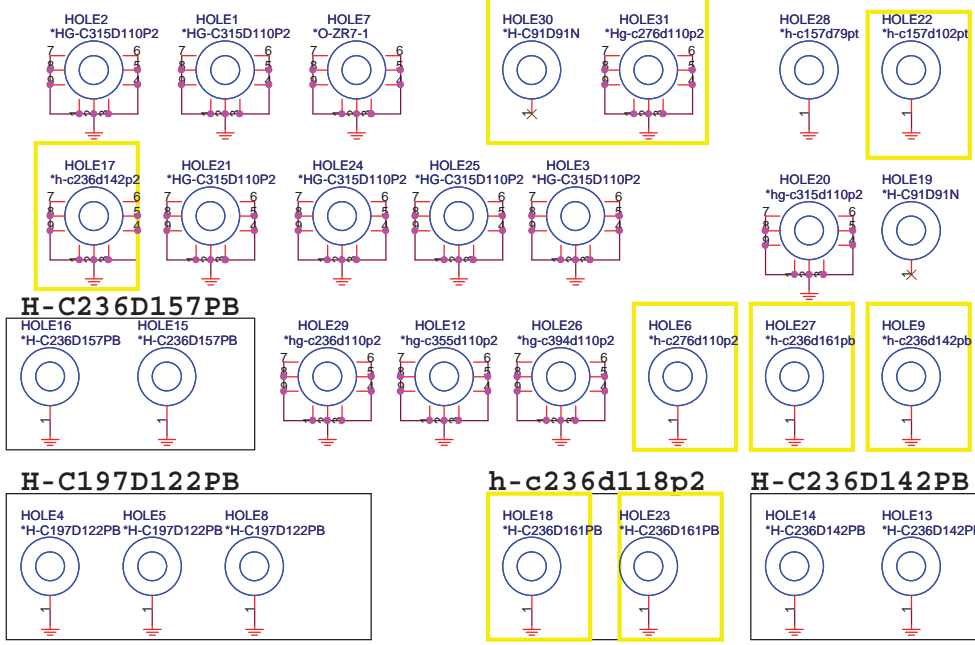
CPU FAN



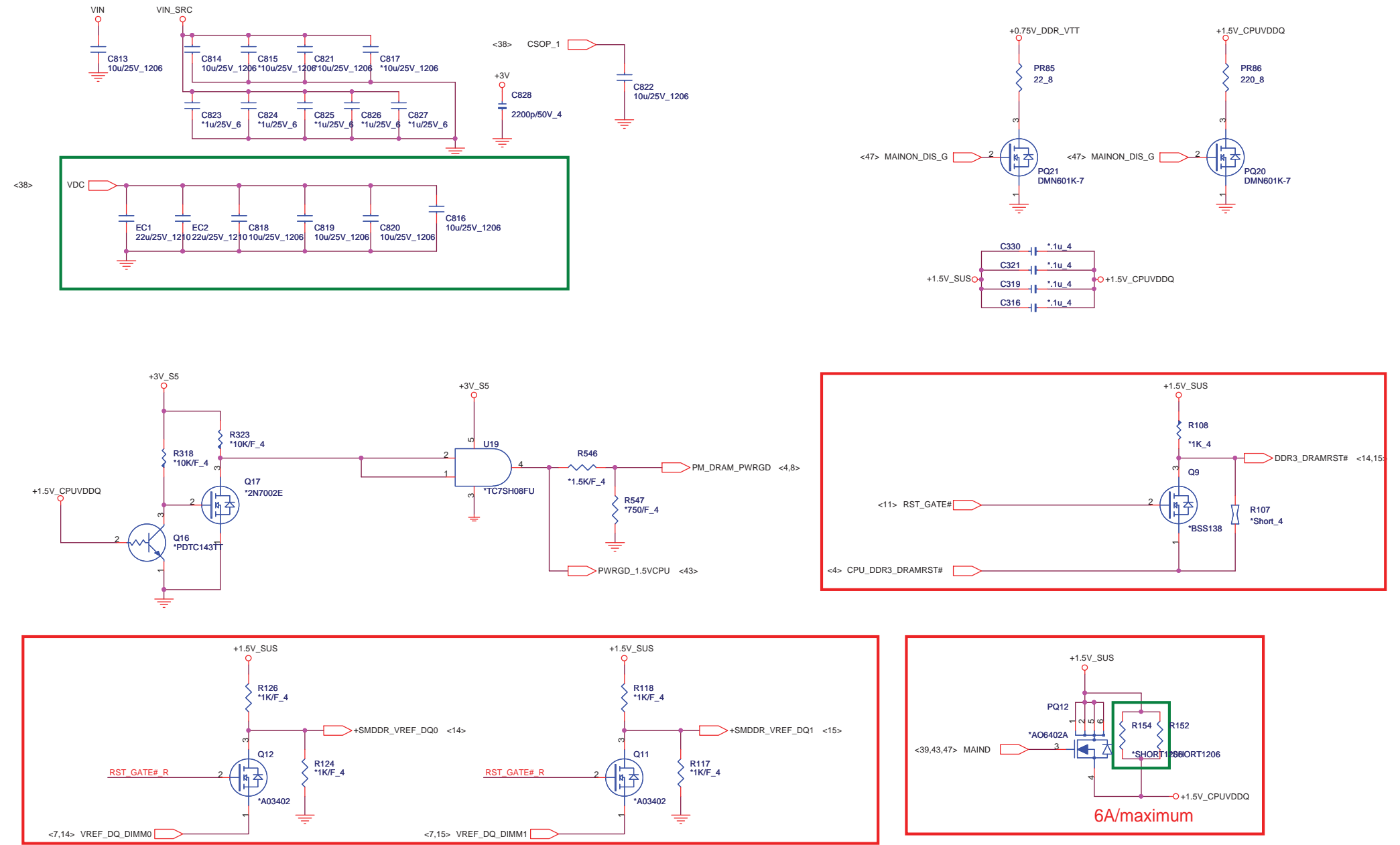
TOUCHPAD & Switch CONN.

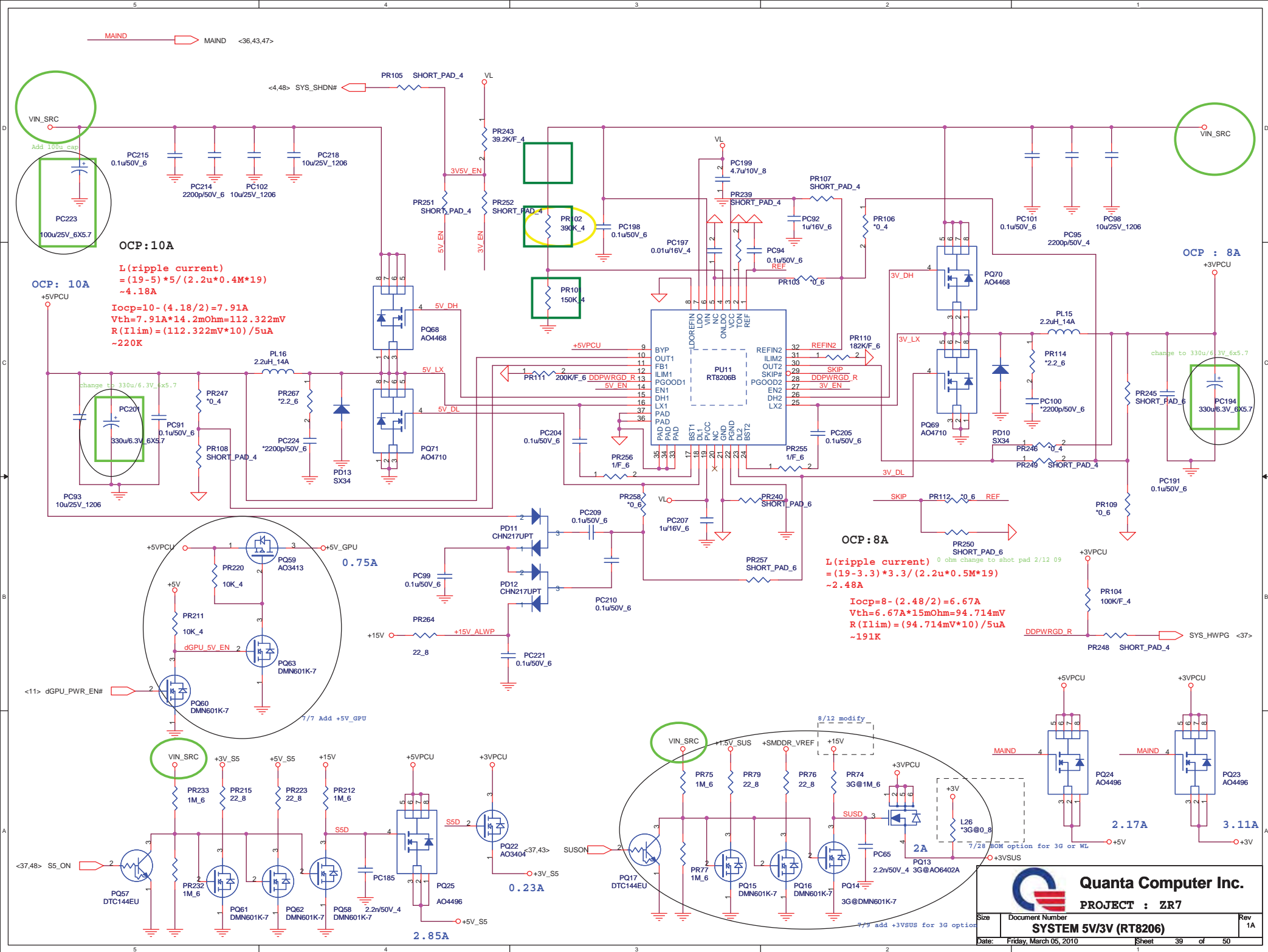


H-C157D63PT



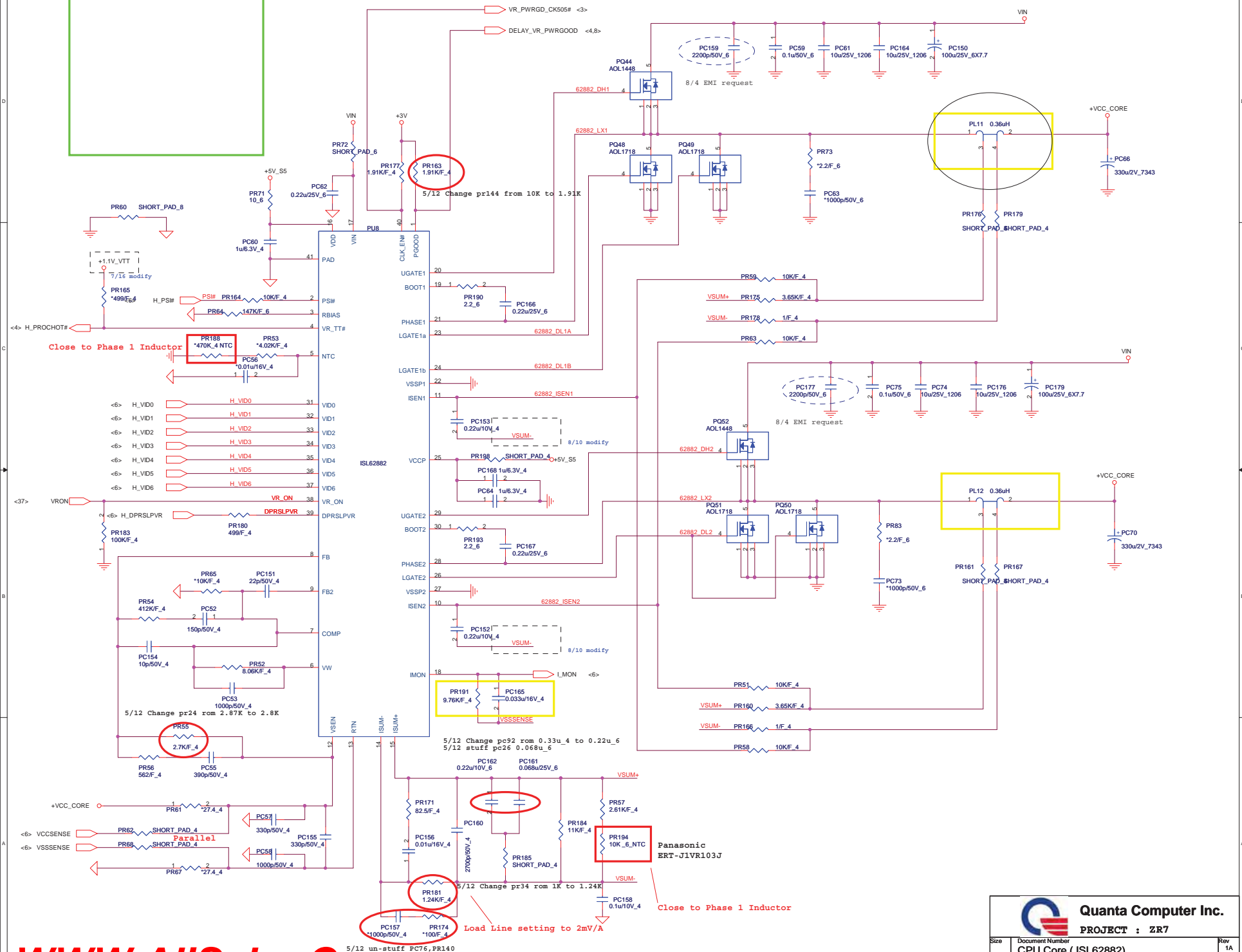
EMI decoupling



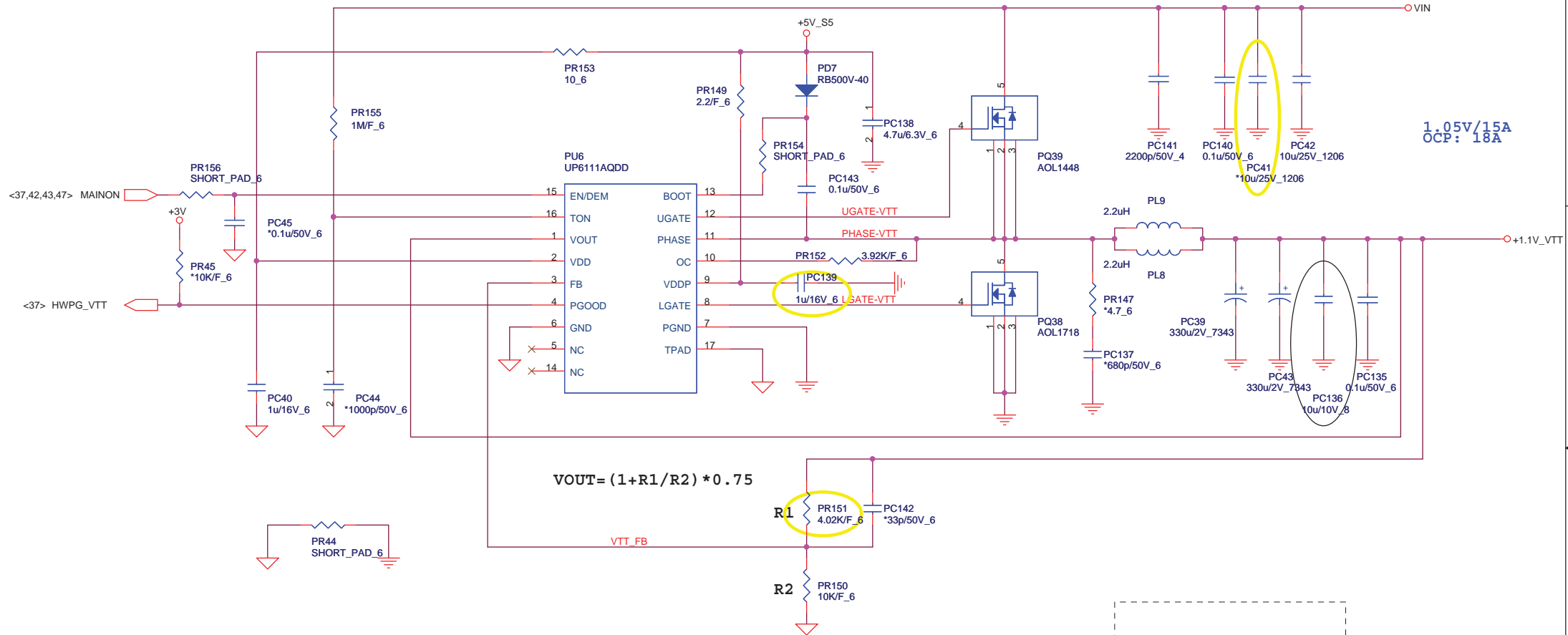


[PWM]

PR71, PR72, PR73, PR74, PR75, PR76, and PR77 deleted



[PWM]



$$TON = 3.85p * RTON * Vout / (Vin - 0.5)$$

$$Frequency = Vout / (Vin * TON)$$

$$TON = 3.85p * 1M * 1 / (Vin - 0.5)$$

$$Frequency = 1 / (0.0036767) = 272K$$

AO1718 Rdson=3~4.3mOhm

$$L(ripple\ current) = (19 - 1.05) * 1.05 / (1u * 272k * 19) \sim 3.64A$$

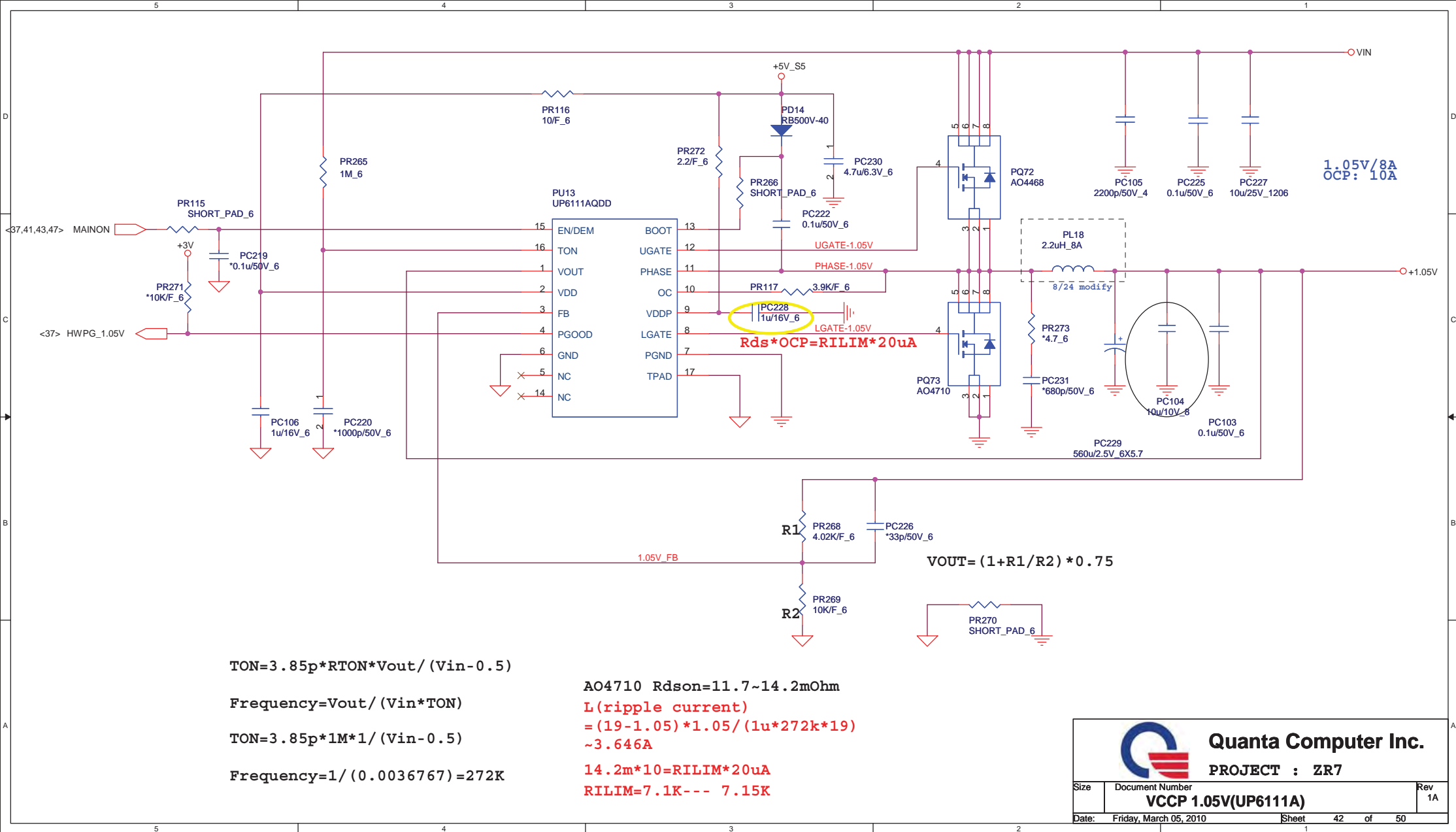
$$4.3m * 18 = RILIM * 20uA$$

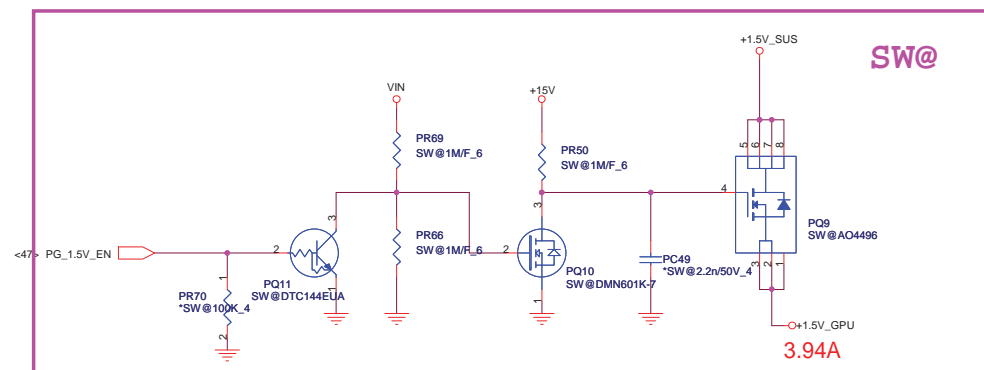
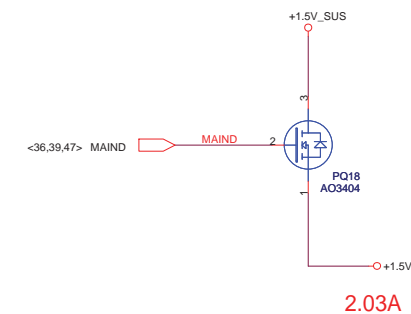
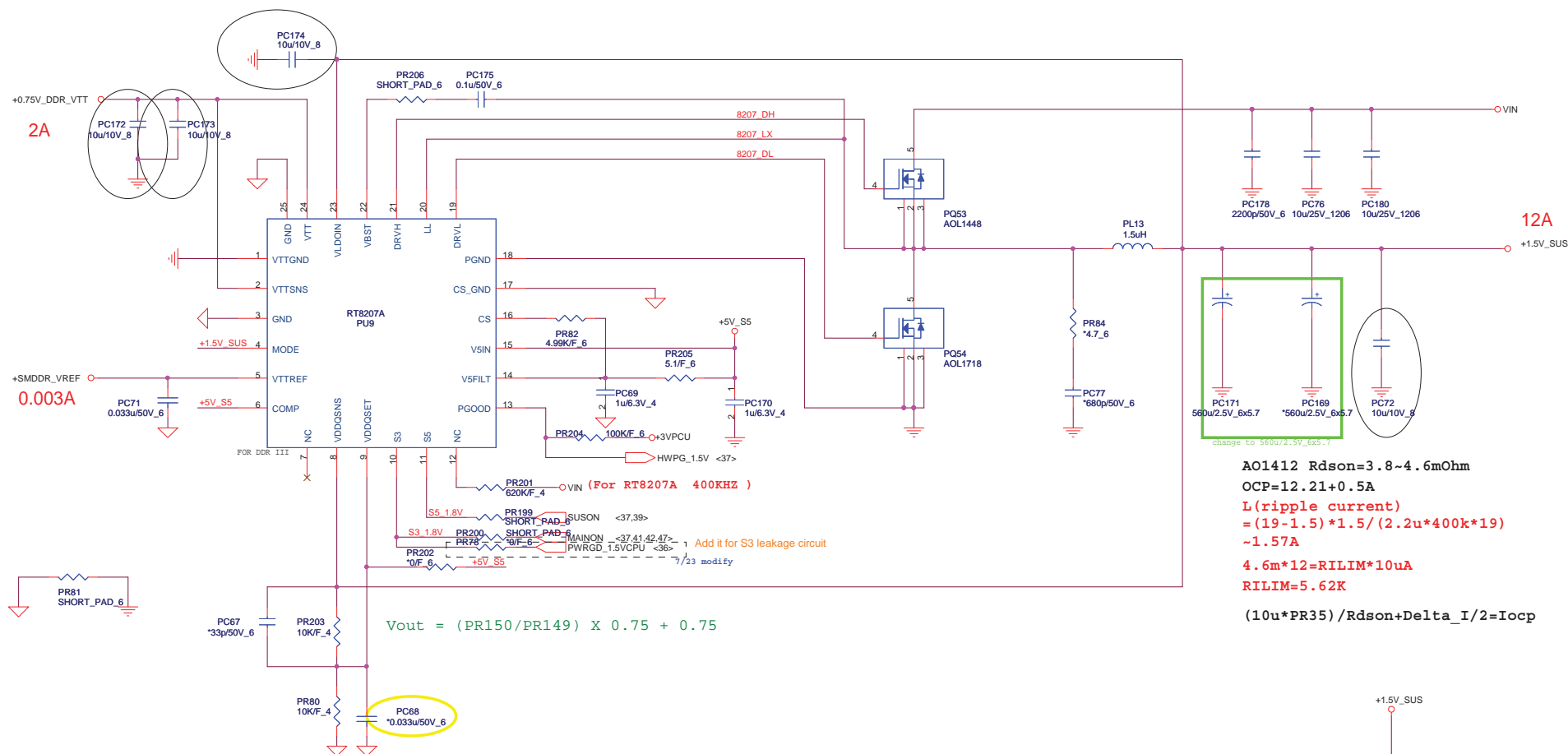
$$RILIM = 3.87K \text{ --- } 3.92K$$

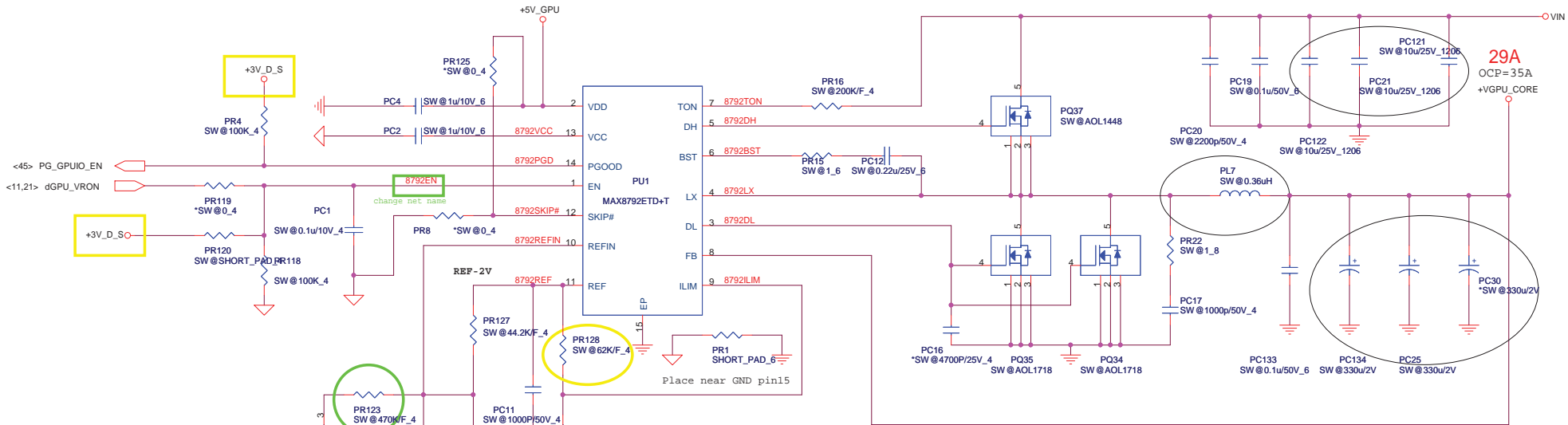


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	+VTT (UP6111A)	1A
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Frequency(PR220=200K) 300K

Madison VID Table

VID1	VID2		+VCC_GFX_CORE
VCORE1.2ID0	VCORE1.2ID1		
LOW (0)	LOW (0)		1.05V
HIGH (1)	LOW (0)		1.0V
LOW (0)	HIGH (1)		0.95V
HIGH (1)	HIGH (1)		0.90V

PR127 = 44.2K
PR129 = 49.9K
PR123 = 470K
PR5 = 220K

PARK VID Table

VID1	VID2		+VCC_GFX_CORE
VCORE1.2ID0	VCORE1.2ID1		
LOW (0)	LOW (0)		1.12V
HIGH (1)	LOW (0)		1.05V
LOW (0)	HIGH (1)		0.95V
HIGH (1)	HIGH (1)		0.90V

PR127 = 39.2K CS33922FB15
PR129 = 49.9K CS43322FB15
PR123 = 332K CS41302FB00
PR5 = 130K

change net name

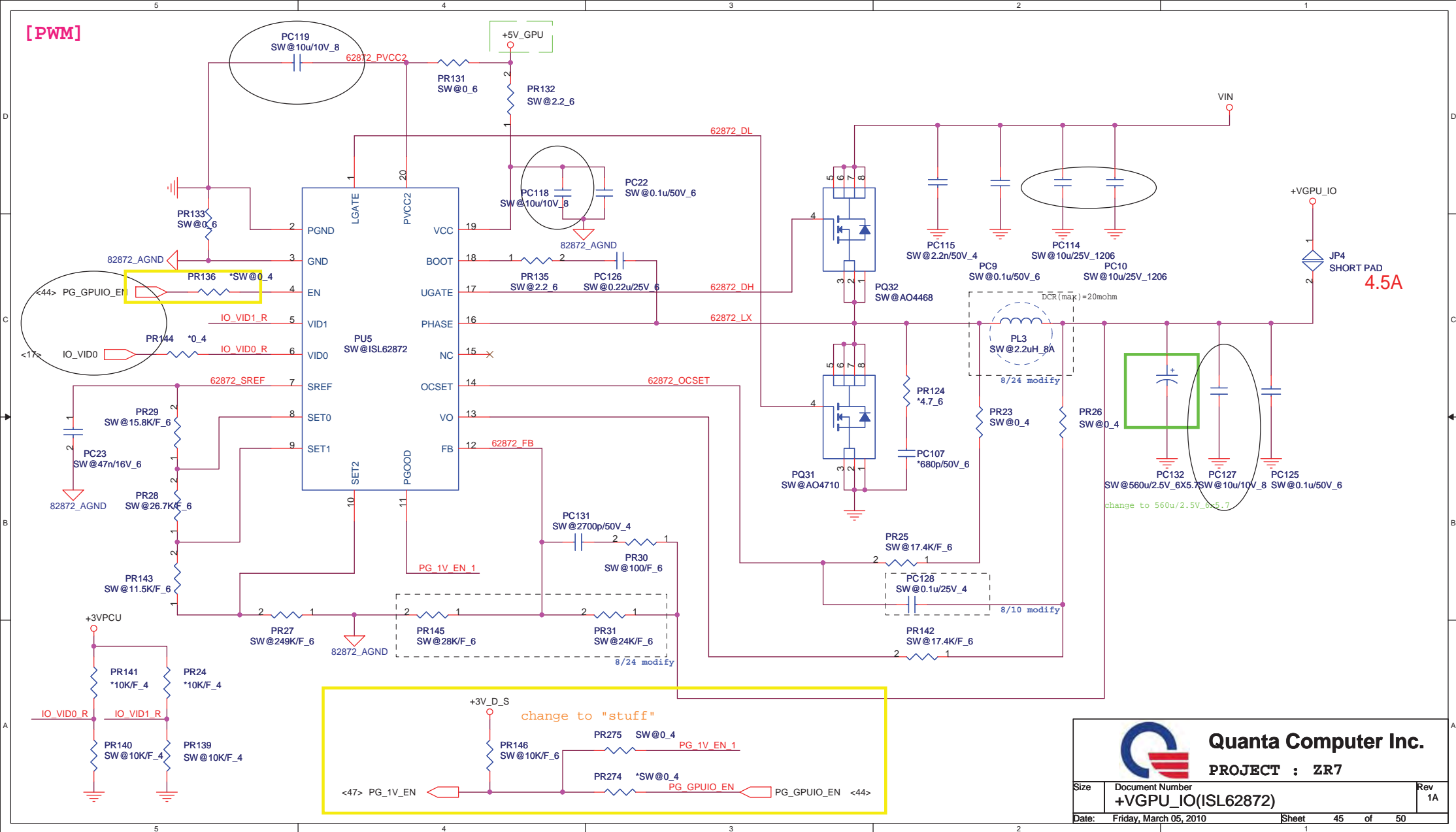
8792EN

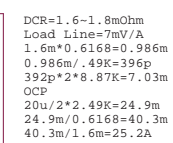
take out PR322

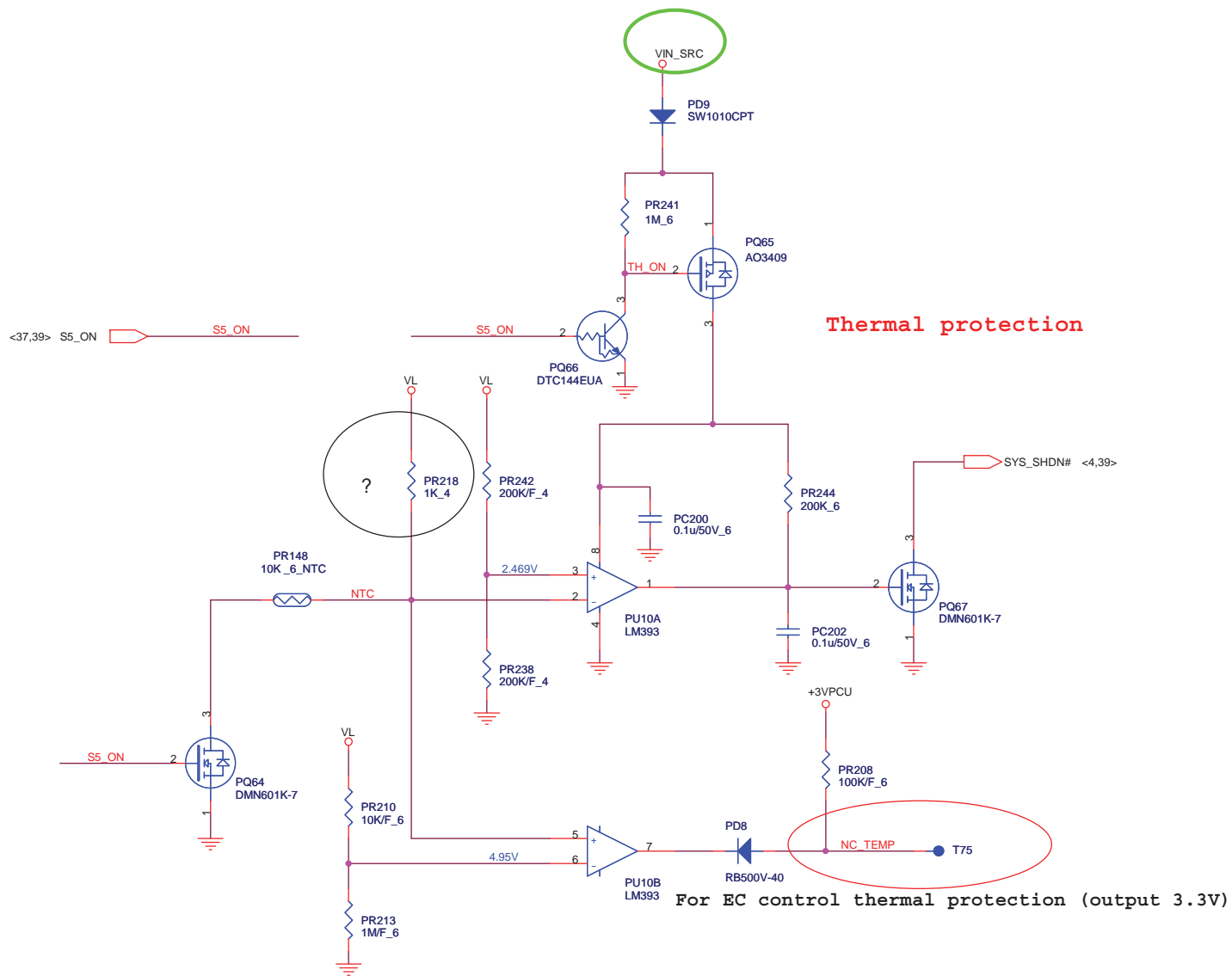


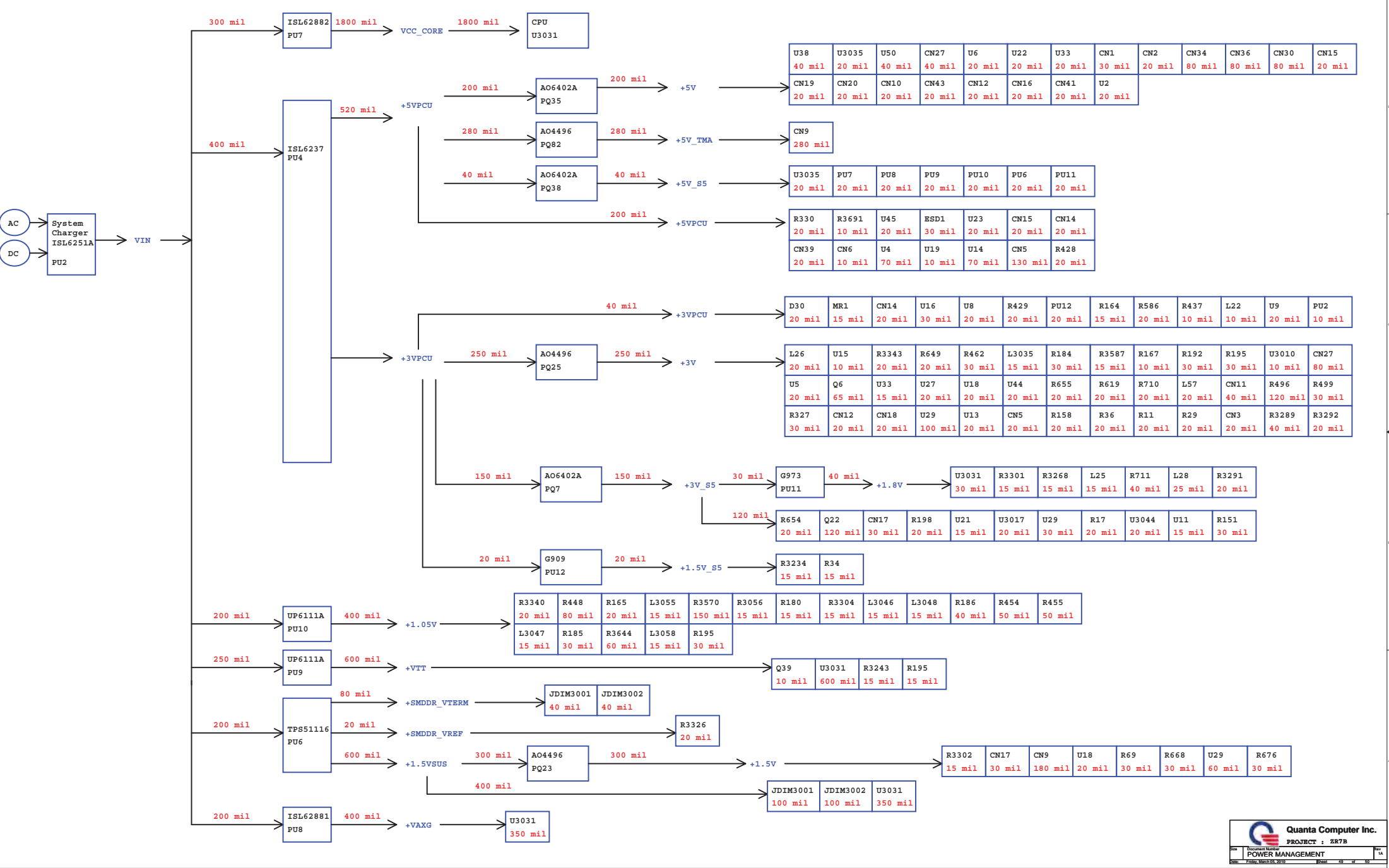
take out PR318, PQ79, PC258, and PR320

[PWM]









[illegible]